



CM85V-24A-3S-Tx-Cx

1.25Gbps 850nm MMF 550m 1x9 Optical Transceiver

Data Sheet



DESCRIPTION

The CM85V-24A-3S-Tx-Cx duplex 1x9 optical transceivers are high performance, cost effective optical transceiver modules for serial optical data communications application specified for a data rate of 1.25Gb/s. The 1x9 transceiver module provides 550m transmission distance over multi-mode fiber at nominal wavelength of 850nm. The optical transceiver is RoHS compliant.

FEATURES

- Compliant with IEEE 802.3 Gigabit Ethernet standard
- Industry standard 1x9 footprint
- SC duplex connector
- Single power supply 3.3V
- Differential inputs and outputs
- Compatible with solder and aqueous wash processes
- Class 1 laser product compliant with EN 60825-1
- Up to 550m over multimode fiber

APPLICATIONS

- 1000Base-SX

ORDERING INFORMATION

PART NUMBER	INPUT/OUTPUT	SIGNAL DETECT	TEMPERATURE	CLIPPER/SHIELD
CM85V-24A-3S-TC-C	AC/AC	LVTTTL	0°C to 70°C	No Shield
CM85V-24A-3S-TC-CB	AC/AC	LVTTTL	0°C to 70°C	Backward Clipper
CM85V-24A-3S-TC-CF	AC/AC	LVTTTL	0°C to 70°C	Forward Clipper
CM85V-24A-3S-TM-C	AC/AC	LVTTTL	-20°C to 85°C	No Shield
CM85V-24A-3S-TM-CB	AC/AC	LVTTTL	-20°C to 85°C	Backward Clipper
CM85V-24A-3S-TM-CF	AC/AC	LVTTTL	-20°C to 85°C	Forward Clipper
CM85V-24A-3S-TI-C	AC/AC	LVTTTL	-40°C to 85°C	No Shield
CM85V-24A-3S-TI-CB	AC/AC	LVTTTL	-40°C to 85°C	Backward Clipper
CM85V-24A-3S-TI-CF	AC/AC	LVTTTL	-40°C to 85°C	Forward Clipper

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T _s	-40	85	°C	
Supply Voltage	V _{CC}	-0.5	4.0	V	
Input Voltage	V _{IN}	-0.5	V _{CC}	V	
Soldering Temperature	T _{SOLD}	-	260	°C	10 seconds on leads

OPERATING ENVIRONMENT

PARAMETER	SYMBOL	MIN	MAX	UNIT
Ambient Operating Temperature	T _{AMB}	0	70	°C
		-20	85	
		-40	85	
Supply Voltage	V _{CC}	3.1	3.5	V
Supply Current	Tx+Rx	-	200	mA

TRANSMITTER ELECTRO-OPTICAL CHARACTERISTICS

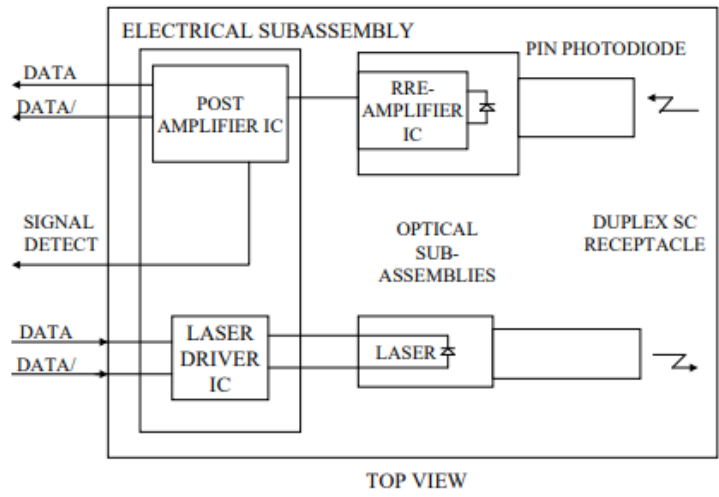
PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Output Optical Power 62.5/125um fiber	P _{out}	-9.5	-	-4	dBm	Average
Output Optical Power 50/125um fiber	P _{out}	-9.5	-	-4	dBm	Average
Extinction Ratio	ER	9	-	-	dB	
Center Wavelength	λ _C	830	850	860	nm	
Spectral Width (RMS)	Δλ	-	-	0.85	nm	
Rise/Fall Time (20~80%)	T _{r,f}	-	-	260	ps	
Relative Intensity Noise	RIN	-	-	-117	dB/Hz	
Total Jitter	TJ	-	-	227	ps	
Output Eye	Compliant with IEEE802.3					
Transmitter Data Input Differential Voltage	V _{DIFF}	0.3	-	2.0	V	

RECEIVER ELECTRO-OPTICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Optical Input Power-Maximum	P _{IN}	0	-	-	dBm	BER<10 ⁻¹²
Optical Input Power-Minimum (Sensitivity)	P _{IN}	-	-	-18	dBm	BER<10 ⁻¹²
Operating Center Wavelength	λ _C	770	-	860	nm	
Optical Return Loss	ORL	12	-	-	dB	
Signal Detect-Asserted	P _A	-	-	-18	dBm	
Signal Detect-Deasserted	P _D	-35	-	-	dBm	
Signal Detect-Hysteresis	P _A -P _D	1.0	-	-	dB	
Stressed Receiver Sensitivity		-	-	-13.5	dBm	50um MMF
		-	-	-12.5		62.5um MMF
Signal Detect Output Voltage-High	V _{OH}	V _{CC} -0.8	-	V _{CC}	V	
Signal Detect Output Voltage-Low	V _{OL}	0	-	0.5	V	
Data Output Rise, Fall time (20~80%)	T _{r,f}	-	-	0.35	ns	
Data Output Differential Voltage	V _{DIFF}	0.6	-	1.2	V	



BLOCK DIAGRAM OF TRANSCEIVER



Transmitter Section - The transmitter section consists of an 850 nm laser in an eye safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a LD driver IC which converts differential input logic signals into an analog laser driving current.

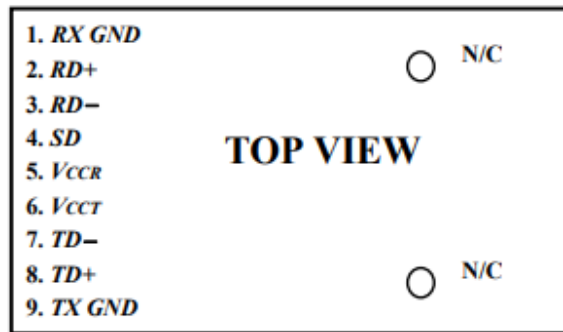
Receiver Section - The receiver utilizes a detector integrated with a trans-impedance preamplifier in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

Receiver Signal Detect - Signal Detect is a basic fiber failure indicator. This is a single-ended LVTTTL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point).



CONNECTION DIAGRAM

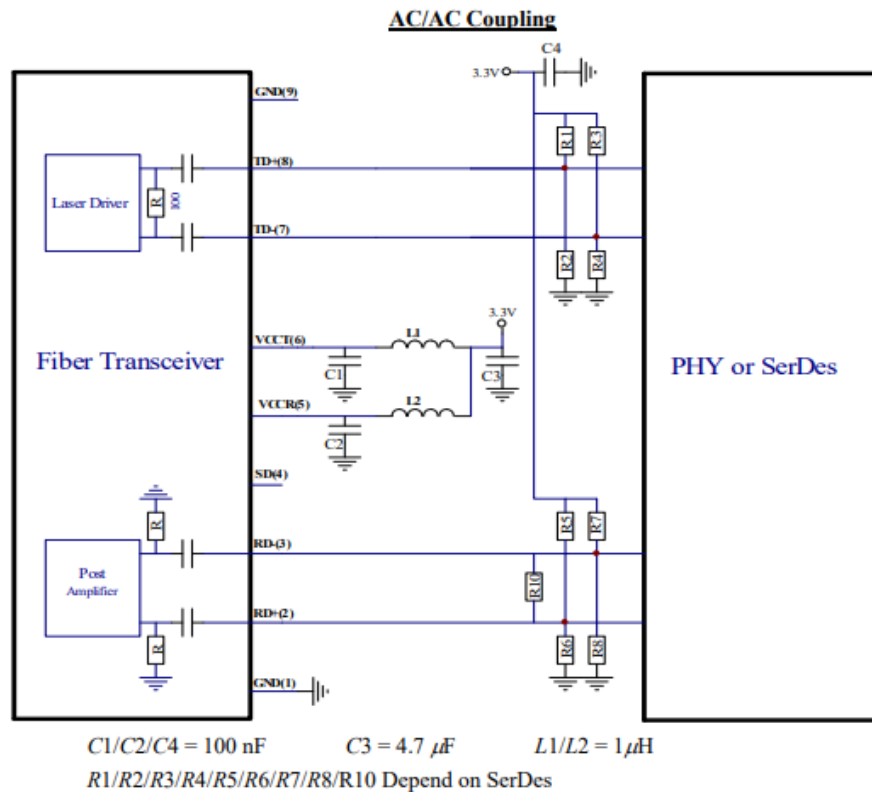
Pin-Out



PIN	SYMBOL	DESCRIPTION
1	<i>RX GND</i>	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	<i>RD+</i>	Receiver Data Output Internally ac coupled. Terminate this differential data output with a 50Ω line and a 50Ω load at the follow-on device (See recommended circuit schematic)
3	<i>RD-</i>	Receiver Data Output-Bar Internally ac coupled. Terminate this differential data output with a 50Ω line and a 50Ω load at the follow-on device (See recommended circuit schematic)
4	<i>SD</i>	Signal Detect. Normal optical input levels to the receiver result in a logic “1” output, <i>V_{OH}</i> , asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic “0” output <i>V_{OL}</i> , deasserted Signal Detect is a LVTTTL output.
5	<i>VCCR</i>	Receiver Power Supply. Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the <i>VCCR</i> pin.
6	<i>VCCR</i>	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the <i>VCCR</i> pin.
7	<i>TD-</i>	Transmitter Data In-Bar. Internally ac coupled. The input stage is internally biased and 50Ω terminated. (See recommended circuit schematic)
8	<i>TD+</i>	Transmitter Data In. Internally ac coupled. The input stage is internally biased and 50Ω terminated. (See recommended circuit schematic)
9	<i>TX GND</i>	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.



RECOMMENDED CIRCUIT SCHEMATIC

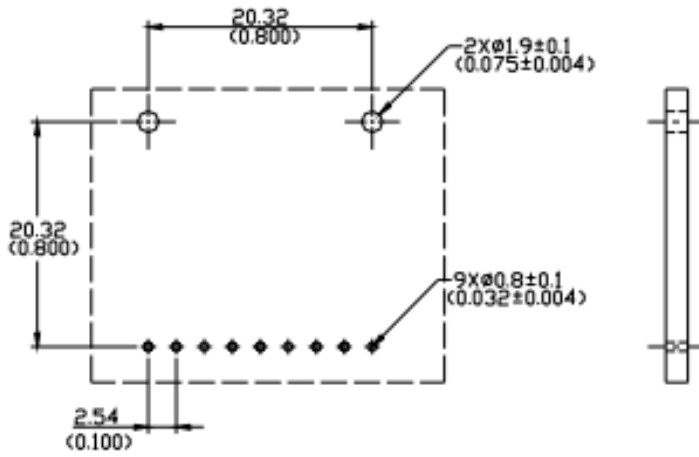


In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic. When designing the circuit interface, there are a few fundamental guidelines to follow.

- (1) The differential data lines should be treated as 50 Ω Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.
- (2) For the high-speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.
- (3) Multi-layer plane PCB is best for distribution of V_{CC}, returning ground currents, forming transmission lines and shielding. Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.
- (4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress V_{CC} noise over a broad frequency range, this prevents receiver sensitivity degradation due to V_{CC} noise.
- (5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1 μF capacitors and a surface-mount coil inductor for 1 μH inductor. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter.
- (6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.



RECOMMENDED BOARD LAYOUT HOLE PATTERN

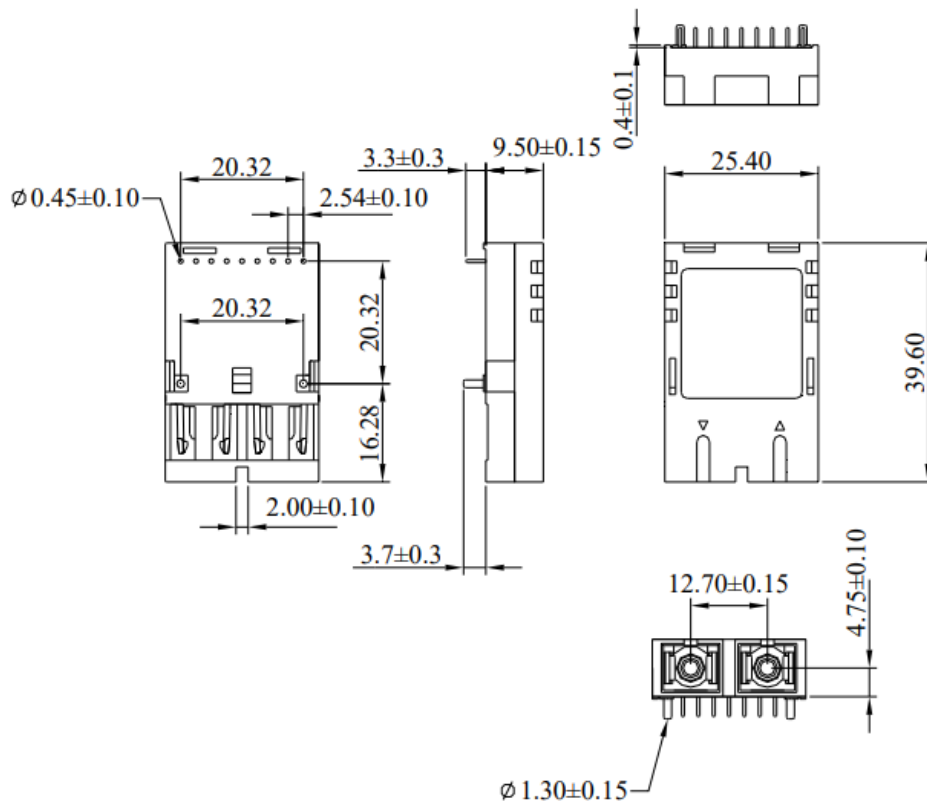


Unit : mm(inches)

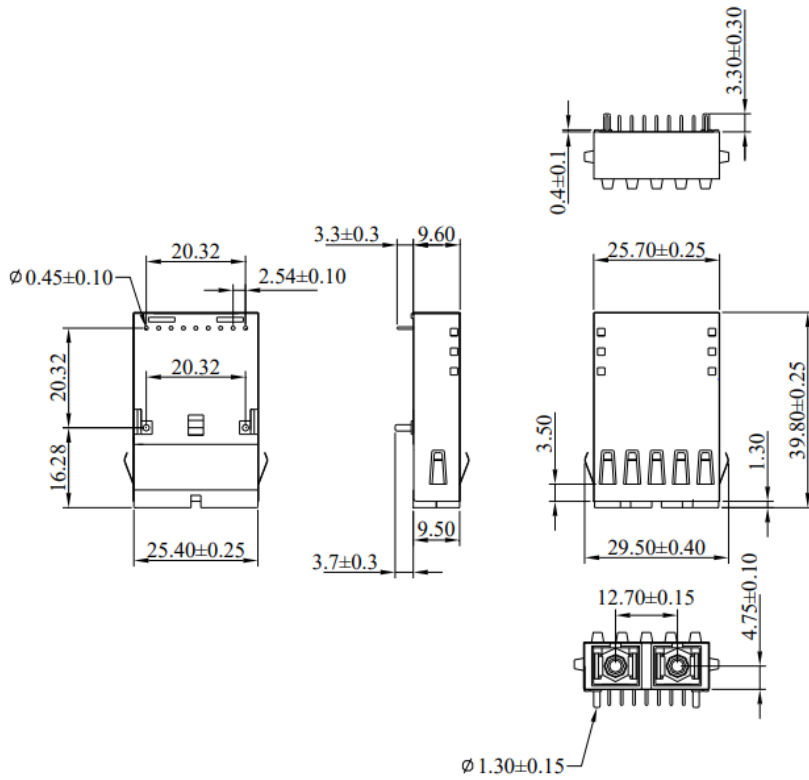
DRAWING DIMENSIONS (unit: mm)

All dimensions are ± 0.20 mm unless otherwise specified.

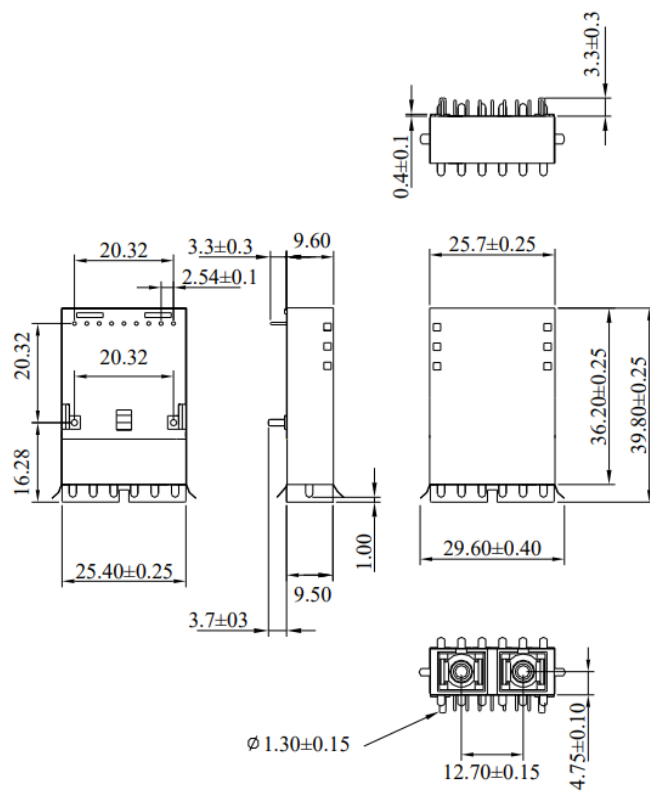
No Shield



Backward Shield



Forward Shield



ADDITIONAL NOTES

- Avoid eye or skin exposure to laser radiations.
- The device is sensitive to electro-static discharge (ESD). The device should be handled with ESD proof tools. To assemble the device on PCB, proper grounding is required to prevent ESD.
- Specifications are subject to change without notice.

