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Data Sheet
Rev 01.1220

155Mbps 1470nm~1610nm SMF 35dB CWDM 2x5 SFF Optical Transceiver with Duplex LC Connector

CS15xxD-03K-3U-PC-L

DESCRIPTION

The CS15xxD-03K-3U-PC-L is a duplex 2x5 SFF (Small Form Factor) CWDM bi-directional optical transceiver designed for data rates up to 155 Mbps over single-mode fiber. It offers a 35 dB power budget and supports eight discrete center wavelengths ranging from 1470 nm to 1610 nm with 20 nm channel spacing, enabling robust medium to long-distance fiber optic communication. The module features a duplex LC connector and provides a cost-effective, high-performance solution for CWDM applications.

FEATURES

- Compliant with 155 Mbps ATM and SONET OC-3 SDH STM-1
- Industry standard 1x9 footprint
- LC duplex connector
- Single power supply 3.3V
- Differential LVPECL inputs and outputs
- Compatible with solder and aqueous wash processes
- Class 1 laser product compliant with EN 60825-1
- Input/Output: DC/DC
- Temperature: 0°C to 70°C
- 35dB power budget

APPLICATIONS

- CWDM Network

PRODUCT OVERVIEW

PART NUMBER	WAVELENGTH
CS1547D-03K-3U-PC-L	1470nm
CS1549D-03K-3U-PC-L	1490nm
CS1551D-03K-3U-PC-L	1510nm
CS1553D-03K-3U-PC-L	1530nm
CS1555D-03K-3U-PC-L	1550nm
CS1557D-03K-3U-PC-L	1570nm
CS1559D-03K-3U-PC-L	1590nm
CS1561D-03K-3U-PC-L	1610nm

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T_S	-40	85	°C	
Supply Voltage	V_{CC}	-0.5	4.0	V	
Input Voltage	V_{IN}	-0.5	V_{CC}	V	
Output Current	I_o	-	50	mA	
Soldering Temperature	T_{SOLD}	-	260	°C	10 seconds on leads

OPERATING ENVIRONMENT

PARAMETER	SYMBOL	MIN	MAX	UNIT
Case Operating Temperature	T_C	0	70	°C
Supply Voltage	V_{CC}	3.1	3.5	V

TRANSMITTER ELECTRO-OPTICAL CHARACTERISTICS (V_{CC} = 3.1V to 3.5V, T_C = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Data Rate	B	50	155	200	Mbps	
Output Optical Power 9/125um fiber	P_{out}	0	-	+5	dBm	Average
Extinction Ratio	ER	10	-	-	dB	
Center Wavelength	λ_C	λ-5.5	λ+1	λ+7.5	nm	
Spectral Width (-20dB)	Δλ	-	-	1	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Rise/Fall Time (10~90%)	$T_{r,f}$	-	1	2	ns	
Output Eye	Compliant with Telcordia GR-253-CORE Issue 3 and ITU-T recommendation G-957					
Power Supply Current	I_{CC}	-	-	140	mA	Note 1
Disable Input Voltage-High	T_{dis}	2.0	-	-	V	
Disable Input Voltage-Low	T_{dis}	-	-	0.8	V	
Transmitter Data Input Voltage-High	V_{IH}-V_{CC}	-1.1	-	-0.74	V	Note 2
Transmitter Data Input Voltage-Low	V_{IL}-V_{CC}	-2.0	-	-1.58	V	Note 2

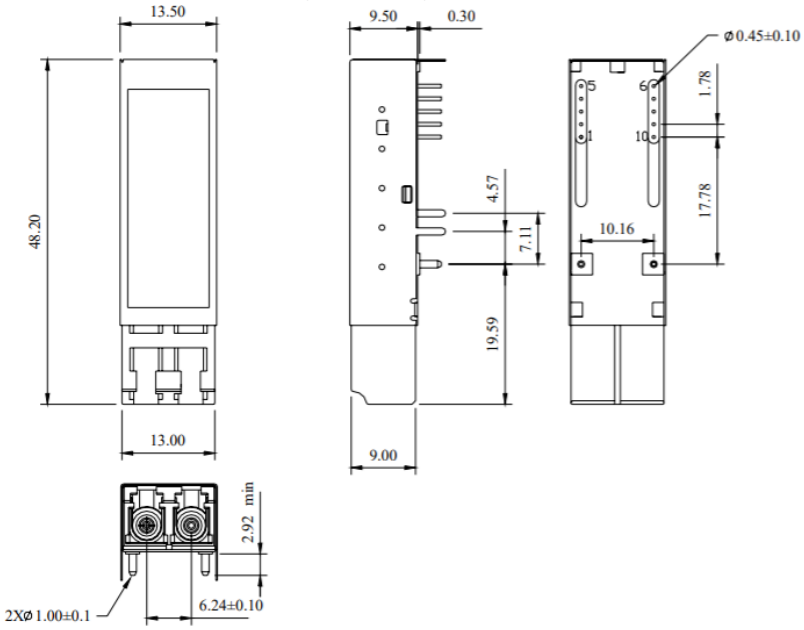
Note 1: Note including the terminations.
Note 2: These inputs are compatible with 10K, 10KH and 100K ECL and PECL input.

RECEIVER ELECTRO-OPTICAL CHARACTERISTICS (V_{CC} = 3.1V to 3.5V, T_C = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Data Rate	B	50	155	200	Mbps	
Optical Input Power-Maximum	P_{IN}	0	-	-	dBm	Note 1
Receiver Input Power-Minimum (Sensitivity)	P_{IN}	-	-	-35	dBm	Note 1
Operating Center Wavelength	λ_C	1260	-	1610	nm	
Signal Detect-Asserted	P_A	-	-	-35	dBm	Average
Signal Detect-Deasserted	P_D	-45	-	-	dBm	Average
Signal Detect-Hysteresis	P_A-P_D	1.0	-	-	dB	
Signal Detect Output Voltage-High	V_{OH}-V_{CC}	-1.1	-	-0.74	V	Note 2
Signal Detect Output Voltage-Low	V_{OL}-V_{CC}	-2.0	-	-1.58	V	Note 2
Power Supply Current	I_{CC}	-	-	100	mA	Note 3
Data Output Rise, Fall time (10~90%)	$T_{r,f}$	-	1	2	ns	
Data Output Voltage-High	V_{OH}-V_{CC}	-1.1	-	-0.74	V	Note 2
Data Output Voltage-Low	V_{OL}-V_{CC}	-2.0	-	-1.58	V	Note 2

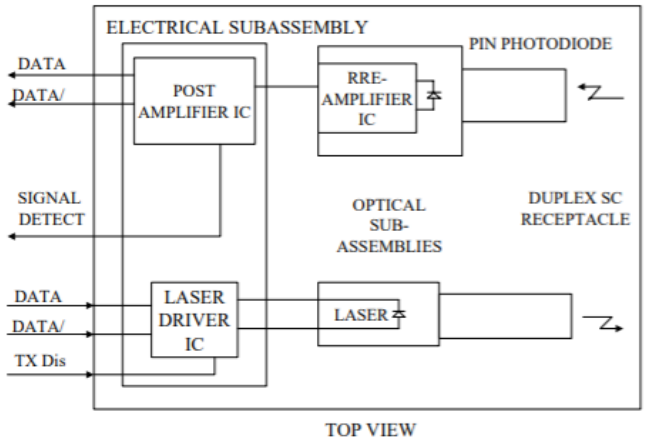
Note 1: The input data is at 155.52 Mbps, 2^{23}–1 PRBS data pattern with 72 “1”s and 72 “0”s inserted per the ITU-T recommendation G.958 Appendix 1. The receiver is guaranteed to provide output data with Bit Error Rate (BER) better than or equal to 1×10^{-10}.
Note 2: These outputs are compatible with 10K, 10KH and 100K ECL and PECL input.
Note 3: The current excludes the output load current.

DRAWING DIMENSIONS (unit: mm)



ALL DIMENSIONS ARE±0.20mm UNLESS OTHERWISE SPECIFIED

BLOCK DIAGRAM OF TRANSCEIVER



TOP VIEW

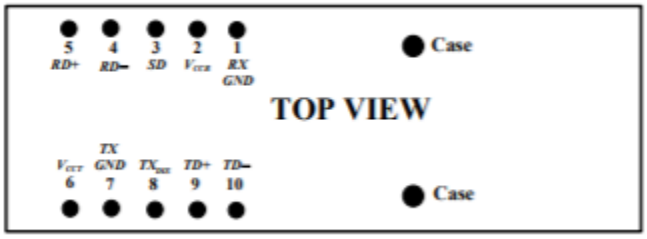
Transmitter Section - The transmitter section consists of a 1550 nm InGaAsP laser in an eye safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a LD driver IC which converts differential input LVPECL logic signals into an analog laser driving current.

Transmitter Disable - Transmitter Disable is a TTL control pin. To disable the module, connect this pin to +3.3 V TTL logic high “1”. To enable module, connect to TTL logic low “0”.

Receiver Section - The receiver utilizes an InGaAs PIN photodiode mounted together with a trans-impedance preamplifier IC in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

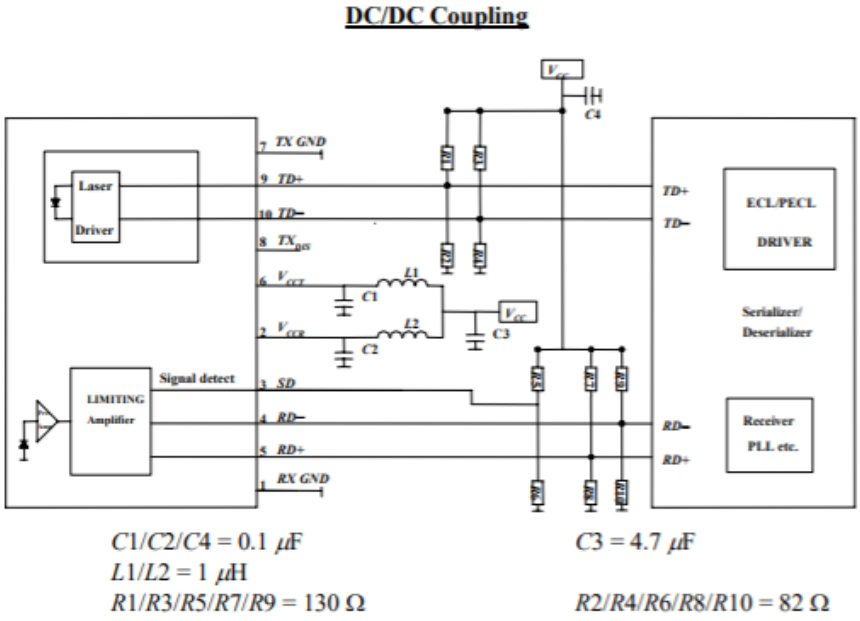
Receiver Signal Detect - Signal Detect is a basic fiber failure indicator. This is a single-ended LVPECL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 1.0 dB higher than the deassert level.

CONNECTION DIAGRAM



PIN	SYMBOL	DESCRIPTION
1	*RX GND*	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	V_{CCR}	Receiver Power Supply Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
3	*SD*	Signal Detect. Normal optical input levels to the receiver result in a logic "1" output, V_{OH}, asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic "0" output V_{OL}, deasserted Signal Detect is a single-ended LVPECL output. *SD* can be terminated with LVPECL techniques via 50Ω to V_{CCR} – 2 V. Alternatively, *SD* can be loaded with a 180 Ω resistor to *RX GND* to conserve electrical power with small compromise to signal quality. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a LVPECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
4	*RD–*	*RD–* is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
5	*RD+*	*RD+* is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
6	V_{CCT}	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	*TX GND*	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.
8	TX_{DIS}	Transmitter Disable. Connect this pin to +3.3V TTL logic high "1" to disable transmitter. To enable module connect to TTL logic low "0" or open.
9	*TD+*	Transmitter Data In Terminate this high-speed differential LVPECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)
10	*TD–*	Transmitter Data In-Bar. Terminate this high-speed differential LVPECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)

RECOMMENDED CIRCUIT SCHEMATIC



In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic. When designing the circuit interface, there are a few fundamental guidelines to follow.

(1) The differential data lines should be treated as 50 Ω Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.

(2) For the high-speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.

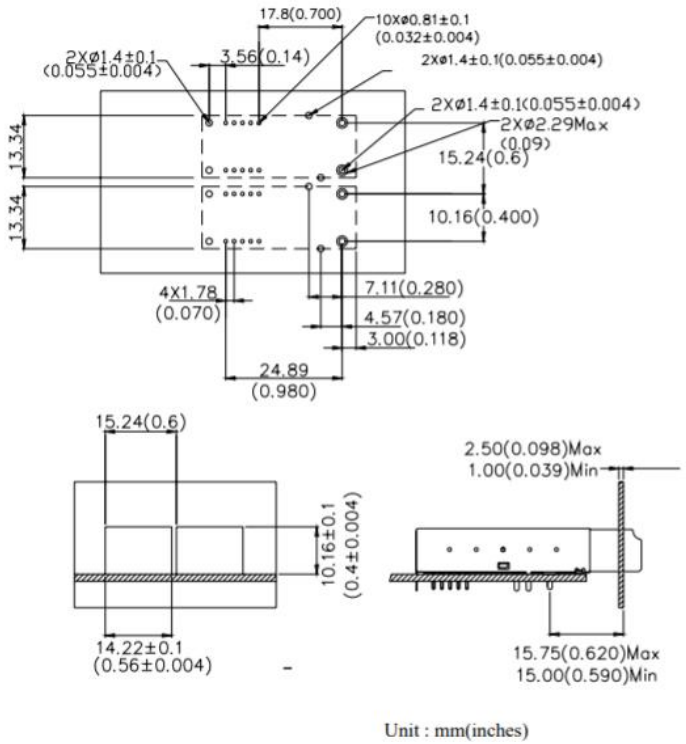
(3) Multi-layer plane PCB is best for distribution of VCC, returning ground currents, forming transmission lines and shielding, Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.

(4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress Vcc noise over a broad frequency range, this prevents receiver sensitivity degradation due to VCC noise.

(5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1 µF capacitors and a surface-mount coil inductor for 1 µH inductor. Ferrite beads can be used to replace the coil inductors when using quieter VCC supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the VCC pins of the receiver and transmitter.

(6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

RECOMMENDED BOARD LAYOUT HOLE PATTERN



Unit : mm(inches)

This transceiver is compatible with industry standard wave or hand solder processes. After wash process, all moisture must be completely removed from the module. The transceiver is supplied with a process plug to prevent contamination during wave solder and aqueous rinse as well as during handling, shipping or storage.

Solder fluxes should be water-soluble, organic solder fluxes. Recommended cleaning and degreasing chemicals for these transceivers are alcohol's (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing.

EYE SAFETY MARK

The single-mode transceiver is a class 1 laser product. It complies with EN 60825-1 and FDA 21 CFR 1040.10 and 1040.11. In order to meet laser safety requirements, the transceiver shall be operated within the Absolute Maximum Ratings.

[Caution] All adjustments have been done at the factory before the shipment of the devices. No maintenance and user serviceable part is required. Tampering with and modifying the performance of the device will result in voided product warranty.

ADDITIONAL NOTES

- Avoid eye or skin exposure to laser radiations.
- The device is sensitive to electro-static discharge (ESD). The device should be handled with ESD proof tools. To assemble the device on PCB, proper grounding is required to prevent ESD.
- Specifications are subject to change without notice.

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