



1.25Gbps 850nm MMF 550m 2x5 SFF Optical Transceiver with Duplex LC Connector

CM85V-24K-3S-Tx-L



DESCRIPTION

The CM85V-24K-3S-Tx-L duplex 2x5 SFF (Small Form Factor) optical transceivers are high performance, cost effective optical transceiver modules for serial optical data communications application specified for a data rate of 1.25Gb/s. The 2x5 SFF transceiver module provides 550m transmission distance over multi-mode fiber at nominal wavelength of 850nm. The optical transceiver is RoHS compliant.

FEATURES

- RoHS compliant
- Compliant with IEEE 802.3z Gigabit Ethernet standard
- Compliant with Fiber Channel standard
- Industry standard 2x5 footprint
- LC duplex connector
- Single power supply 3.3V
- Class 1 laser product compliant with EN 60825-1
- Input/Output: AC/AC
- Signal Detect: LVTTTL
- Up to 550m over multimode fiber

APPLICATIONS

- 1000Base-SX

PRODUCT OVERVIEW

PART NUMBER	OPERATING TEMPERATURE
CM85V-24K-3S-TC-L	0°C to 70°C
CM85V-24K-3S-TM-L	-10°C to 85°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T _S	-40	85	°C	
Supply Voltage	V _{CC}	-0.5	4.0	V	
Input Voltage	V _{IN}	-0.5	V _{CC}	V	
Operating Current	I _{OP}	-	400	mA	
Soldering Temperature	T _{SOLD}	-	260	°C	10 seconds on leads

OPERATING ENVIRONMENT

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Case Operating Temperature	T _C	0	70	°C	CM85V-24K-3S-TC-L
		-10	85		CM85V-24K-3S-TM-L
Supply Voltage	V _{CC}	3.1	3.5	V	
Supply Current	I _{CC}	-	200	mA	

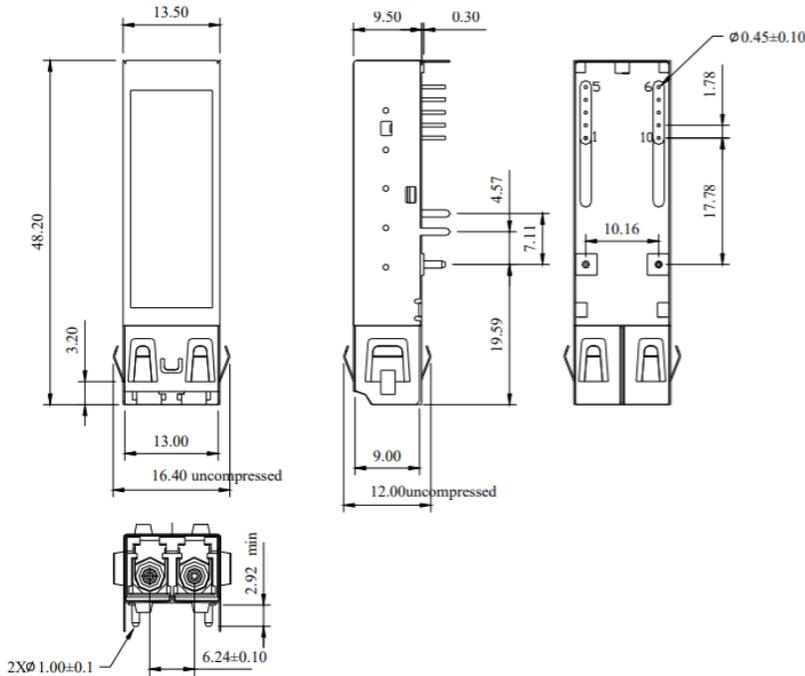
TRANSMITTER ELECTRO-OPTICAL CHARACTERISTICS (V_{CC} = 3.1V to 3.5V, T_C = 0°C to 70°C, -10°C to 85°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Output Optical Power 62.5/125um fiber	P _{out}	-9.5	-	-4	dBm	
Output Optical Power 50/125um fiber	P _{out}	-9.5	-	-4	dBm	
Extinction Ratio	ER	9	-	-	dB	
Center Wavelength	λ _C	830	850	860	nm	
Spectral Width (RMS)	Δλ	-	-	0.85	nm	
Rise/Fall Time (20~80%)	T _{r,f}	-	-	260	ps	
Relative Intensity Noise	RIN	-	-	-117	dB/Hz	
Total Jitter	TJ	-	-	227	ps	
Output Eye	Compliant with IEEE802.3z					
Max. P _{out} TX-DISABLE Asserted	P _{OFF}	-	-	-45	dBm	
Disable Input Voltage-High	T _{dis-H}	2.2	-	-	V	
Disable Input Voltage-Low	T _{dis-L}	-	-	0.6	V	
Transmitter Data Input Differential Voltage	V _{DIFF}	0.4	-	2.0	V	

RECEIVER ELECTRO-OPTICAL CHARACTERISTICS (V_{CC} = 3.1V to 3.5V, T_C = 0°C to 70°C, -10°C to 85°C)

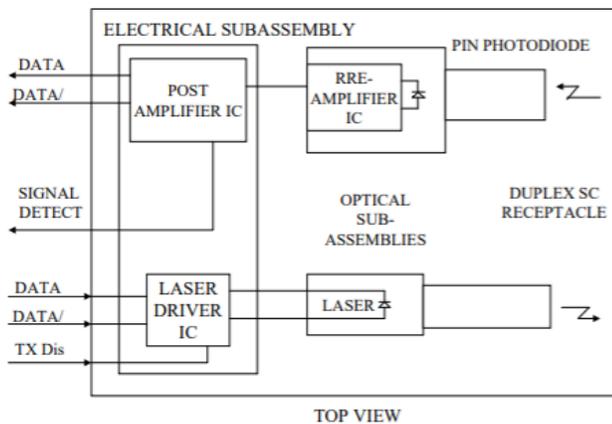
PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Optical Input Power-Maximum	P _{IN}	0	-	-	dBm	BER<10 ⁻¹²
Optical Input Power-Minimum (Sensitivity)	P _{IN}	-	-	-18	dBm	BER<10 ⁻¹²
Operating Center Wavelength	λ _C	770	-	860	nm	
Optical Return Loss	ORL	12	-	-	dB	
Signal Detect-Asserted	P _A	-	-	-18	dBm	
Signal Detect-Deasserted	P _D	-35	-	-	dBm	
Signal Detect-Hysteresis	P _A -P _D	1.0	-	-	dB	
Signal Detect Voltage-High	V _{OH}	2.4	-	V _{CC}	V	
Signal Detect Voltage-Low	V _{OL}	0	-	0.5	V	
Data Output Rise, Fall time (20~80%)	T _{r,f}	-	-	0.35	ns	
Data Output Differential Voltage	V _{DIFF}	0.5	-	1.8	V	

DRAWING DIMENSIONS (unit: mm)



ALL DIMENSIONS ARE ±0.20mm UNLESS OTHERWISE SPECIFIED

BLOCK DIAGRAM OF TRANSCEIVER

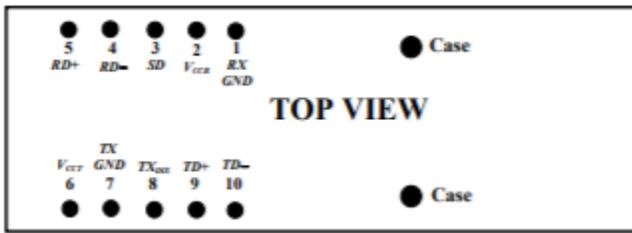


Transmitter Section - The transmitter section consists of a 850 nm laser in an eye safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a LD driver IC which converts differential input LVPECL logic signals into an analog laser driving current.

Receiver Section - The receiver utilizes a MSM detector integrated with a trans-impedance preamplifier in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

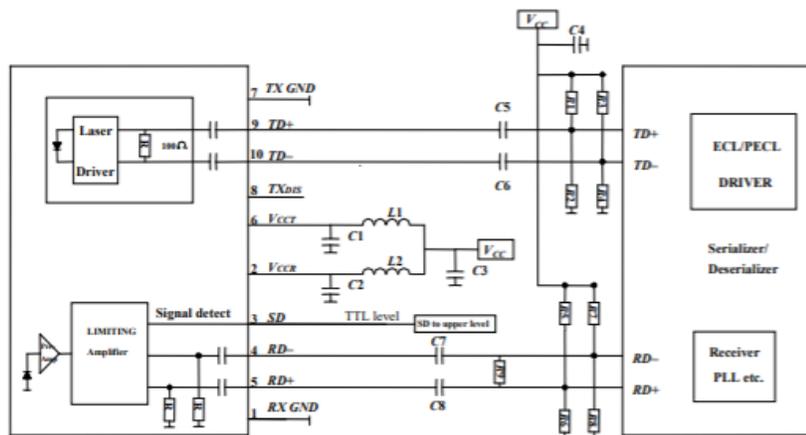
Receiver Signal Detect - Signal Detect is a basic fiber failure indicator. This is a single-ended LVTTTL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 1.0 dB higher than the deassert level.

CONNECTION DIAGRAM



PIN	SYMBOL	DESCRIPTION
1	<i>RX GND</i>	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	<i>VCCR</i>	Receiver Power Supply Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the <i>VCCR</i> pin.
3	<i>SD</i>	Signal Detect. Normal optical input levels to the receiver result in a logic “1” output, <i>V_{OH}</i> , asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic “0” output <i>V_{OL}</i> , deasserted. Signal Detect is a single-ended LVTTTL output.
4	<i>RD-</i>	Receiver Data Output-Bar Internally ac coupled (100nF). Terminate this differential data output with a 50Ω line and a 50Ω load at the follow-on device (See recommended circuit schematic)
5	<i>RD+</i>	Receiver Data Output Internally ac coupled (100nF). Terminate this differential data output with a 50Ω line and a 50Ω load at the follow-on device (See recommended circuit schematic)
6	<i>VCCR</i>	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the <i>VCCR</i> pin.
7	<i>TX GND</i>	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.
8	<i>TXDIS</i>	Transmitter Disable. Connect this pin to +3.3V TTL logic high “1” to disable transmitter. To enable module connect to TTL logic low “0” or open.
9	<i>TD+</i>	Transmitter Data In. Requires an ac coupled input. The input stage is internally biased and 50Ω terminated. (See recommended circuit schematic)
10	<i>TD-</i>	Transmitter Data In-Bar. Requires an ac coupled input. The input stage is internally biased and 50Ω terminated. (See recommended circuit schematic)

RECOMMENDED CIRCUIT SCHEMATIC



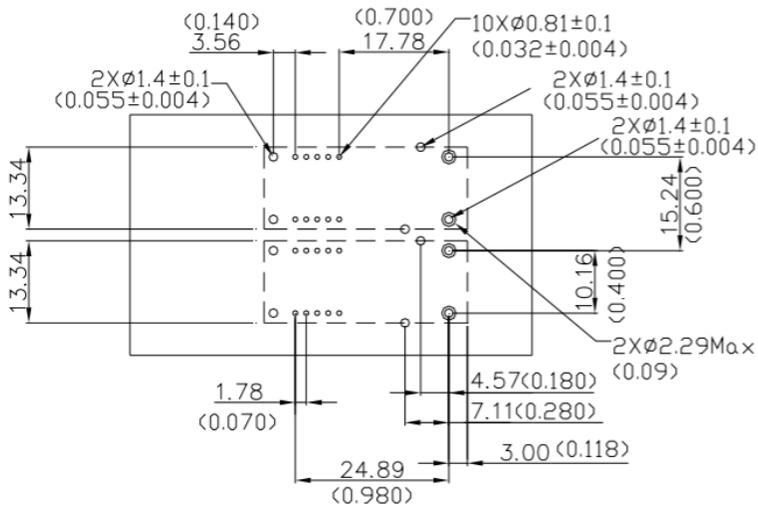
$C1/C2/C4/C5/C6/C7/C8 = 100 \text{ nF}$ $C3 = 4.7 \text{ } \mu\text{F}$ $L1/L2 = 1 \text{ } \mu\text{H}$

$R1/R2/R3/R4/R5/R6/R7/R8/R9$ Depend on SerDes

In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic. When designing the circuit interface, there are a few fundamental guidelines to follow.

- (1) The differential data lines should be treated as 50 Ω Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.
- (2) For the high-speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.
- (3) Multi-layer plane PCB is best for distribution of VCC, returning ground currents, forming transmission lines and shielding, Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.
- (4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress Vcc noise over a broad frequency range, this prevents receiver sensitivity degradation due to VCC noise.
- (5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1 μF capacitors and a surface-mount coil inductor for 1 μH inductor. Ferrite beads can be used to replace the coil inductors when using quieter VCC supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the VCC pins of the receiver and transmitter.
- (6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

RECOMMENDED BOARD LAYOUT HOLE PATTERN



Unit : mm(inches)

ADDITIONAL NOTES

- Avoid eye or skin exposure to laser radiations.
- The device is sensitive to electro-static discharge (ESD). The device should be handled with ESD proof tools. To assemble the device on PCB, proper grounding is required to prevent ESD.
- Specifications are subject to change without notice.



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