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Data Sheet
Rev 01.1220

40GBASE-LR4 SMF 10km 1310nm CWDM QSFP+ Optical Transceiver with Duplex LC Connector

40GSLRSFPC

DESCRIPTION

The 40GSLRSFPC QSFP+ 40GBASE-LR4 transceiver is a new high-speed module with a LC connector. This interconnecting module offers 4 channels and maximum bandwidth of 40Gbps. The optical transceiver module consists of 4x10Gbps CWDM LDs and multiplex 4 CWDM signals on a 40Gbps optical transmission, and de-multiplex 40G receiver signals to 4 CWDM signals.

FEATURES

- Compliant with 40G Ethernet IEEE 802.3ba
- Power dissipation < 3.5W
- Full Digital Diagnostics Monitor Interface
- Up to 10km transmission on SMF
- RoHS-6 Compliant (lead-free)
- Class 1 Laser Product compliant with IEC/EN60825-1: 2007 and IEC/EN60825-1: 2014

APPLICATIONS

- 40G Ethernet
- OTN OTU3
- Data Center Interconnect
- 40GBASE-LR4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Storage Temperature	T_S	-40	85	°C
Supply Voltage	V_{CC}	-0.5	3.6	V
Relative Humidity	RH	5	85	%

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Case Temperature	T_C	0		70	°C
Power Supply Voltage	V_{CC}	3.135	3.3	3.47	V
Power Dissipation				3.5	W

DIAGNOSTICS

PARAMETER	RANGE	ACCURACY	UNIT	CALIBRATION
Temperature	-5 to 75	±5	°C	Internal
Voltage	3.0 to 3.6	±0.1	V	
Bias Current	15 to 70	±10%	mA	
TX Power	-7 to +2.3	±3 dB	dBm	
RX Power	-14.4 to 2.5	±3 dB	dBm	

TRANSMITTER OPTICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Total Average Launch Power	Pt			8.3	dBm	
Extinction Ratio	ER	3.5			dB	
Center Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5		
	L2	1304.5	1311	1317.5		
	L3	1324.5	1331	1337.5		
Average Output Power	P_O	-7		2.3	dBm	1
Optical Modulation Amplitude, per lane	OMA	-4		3.5	dBm	
Difference in Power between any Two Lanes				6.5	dB	
Side Mode Suppression	SMSR	30			dB	
Relative Intensity Noise	RIN20OMA			-128	dB/Hz	
Transmitter Reflectance	R_T			-12	dB	
Transmitter and Dispersion Penalty	TDP			2.3	dB	
Differential Input Voltage	V_{DIFF}	0.2	-	0.8	V	
Disable Output Power	P_{o_off}			-30	dBm	
Output Eye Mask		Compliant with IEEE 802.3ba				

Note 1: Minimum value is informative.

RECEIVER OPTICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Damage Threshold, per lane	Pth	3.3			dBm	
Average Power at Receiver Input, per lane	P_{IN}	-13.7		2.3	dBm	
Receiver Power (OMA), per lane				3.5	dBm	
Receiver Sensitivity (OMA), per lane	Rsens			-11.5	dBm	
Stressed Receiver Sensitivity, per lane				-9.6	dBm	
Differential Input Voltage	V_{DIFF}	0.4	-	0.85	V	
LOS Assert	LOS_A	-28			dBm	1
LOS De-Assert	LOS_D			-15	dBm	1
Receiver Electrical 3dB Upper Cutoff Frequency				12	GHz	
Hysteresis	Hys	0.5		6	dB	
Receiver Reflectance	R_R			-26.0	dB	

Note 1: Average power, Rx output will not be squelched if LOS asserted.

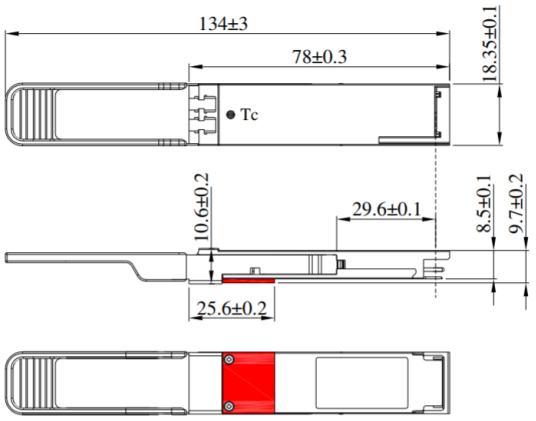
ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Data Rate, per lane			10.3125		Gbps	
LP Mode/Reset/ModselL	VIL	0		0.8	V	
LP Mode/Reset/ModselL	VIH	2		V_{CC}+0.3	V	
ModPrsL/IntL	VOL	0		0.4	V	
ModPrsL/IntL	VOH	2		V_{CC}+0.3	V	

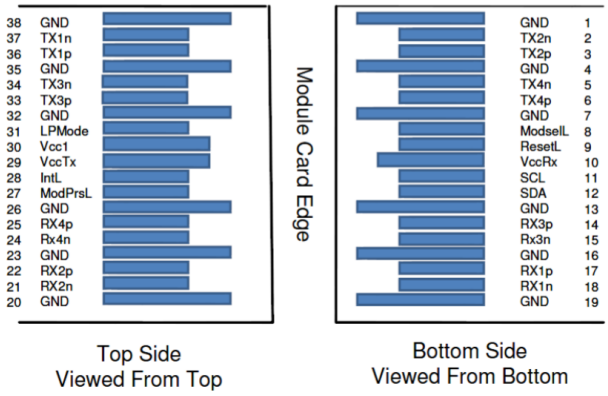
TIMING FOR SOFT CONTROL/STATUS FUNCTION/SQUELCH & DISABLE

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Initialization Time	T_init			2000	ms
Reset Init Assert Time	T_reset_init			2	us
Serial Bus Hardware Ready Time	T_serial			2000	ms
Monitor Data Ready Time	T_data			2000	ms
Reset Assert Time	T_seset			2000	ms
LP Mode Assert Time	Ton_LPMode			100	us
LP Mode Deassert Time	Toff_LPMode			300	ms
IntL Assert Time	Ton_IntL			200	ms
IntL Deassert Time	Toff_IntL			500	us
Rx LOS Assert Time	Ton_los			100	ms
Tx Fault Assert Time	Ton_Txfault			200	ms
Flag Assert Time	Ton_flag			200	ms
Tx Squelch Assert Time	Ton_Txsq			400	ms
Tx Squelch Deassert Time	Toff_Txsq			400	ms
Tx Disable Assert Time	Ton_Txdis			100	ms
Tx Disable Deassert Time	Toff_Txdis			400	ms

DIMENSIONS (unit: mm)



PAD ASSIGNMENT AND DESCRIPTION



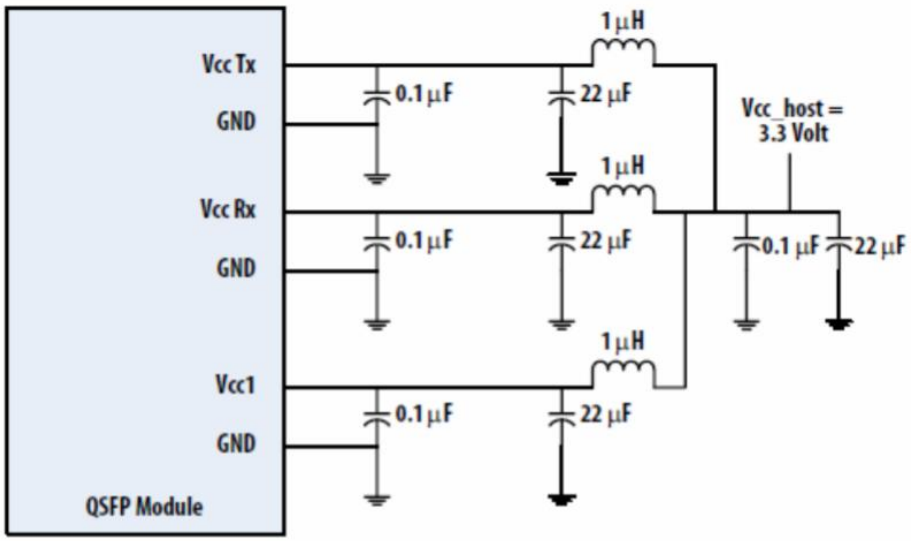
"PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
1		GND	Ground	1	Note 1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	Note 1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	Note 1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	Note 2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	Note 2
14	CML-O	Rx3p	Receiver Non- Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	Note 1
17	CML-O	Rx1p	Receiver Non- Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	

19		GND	Ground	1	Note 1
20		GND	Ground	1	Note 1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2P	Receiver Non- Inverted Data Output	3	
23		GND	Ground	1	Note 1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non- Inverted Data Output	3	
26		GND	Ground	1	Note 1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29	LVCMOS-I/O	Vcc Tx	+3.3V Power Supply transmitter	2	Note 2
30		Vcc1	+3.3V Power Supply	2	Note 2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	Note 1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	Note 1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	Note 1

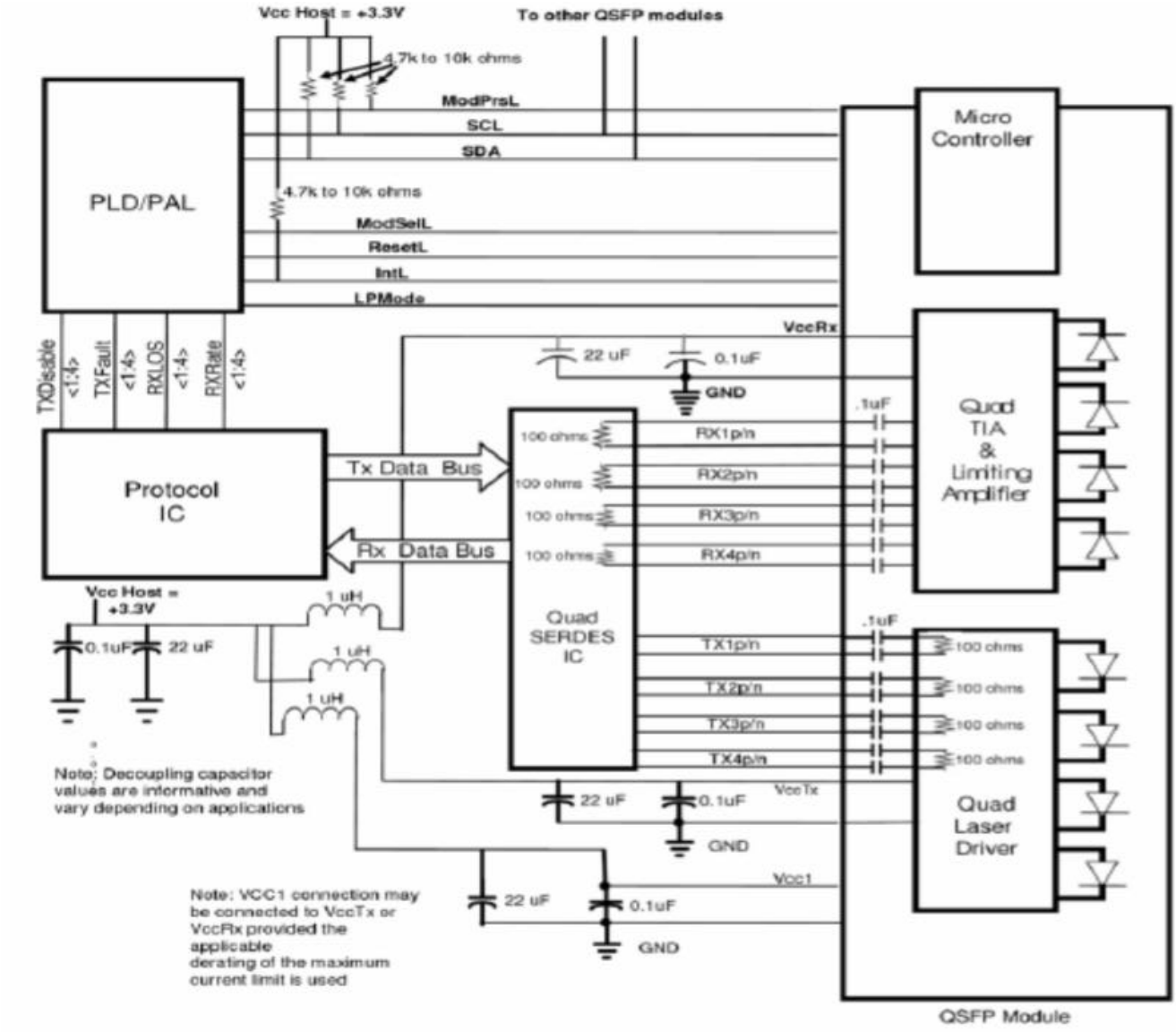
Note 1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

HOST BOARD POWER SUPPLY CIRCUIT

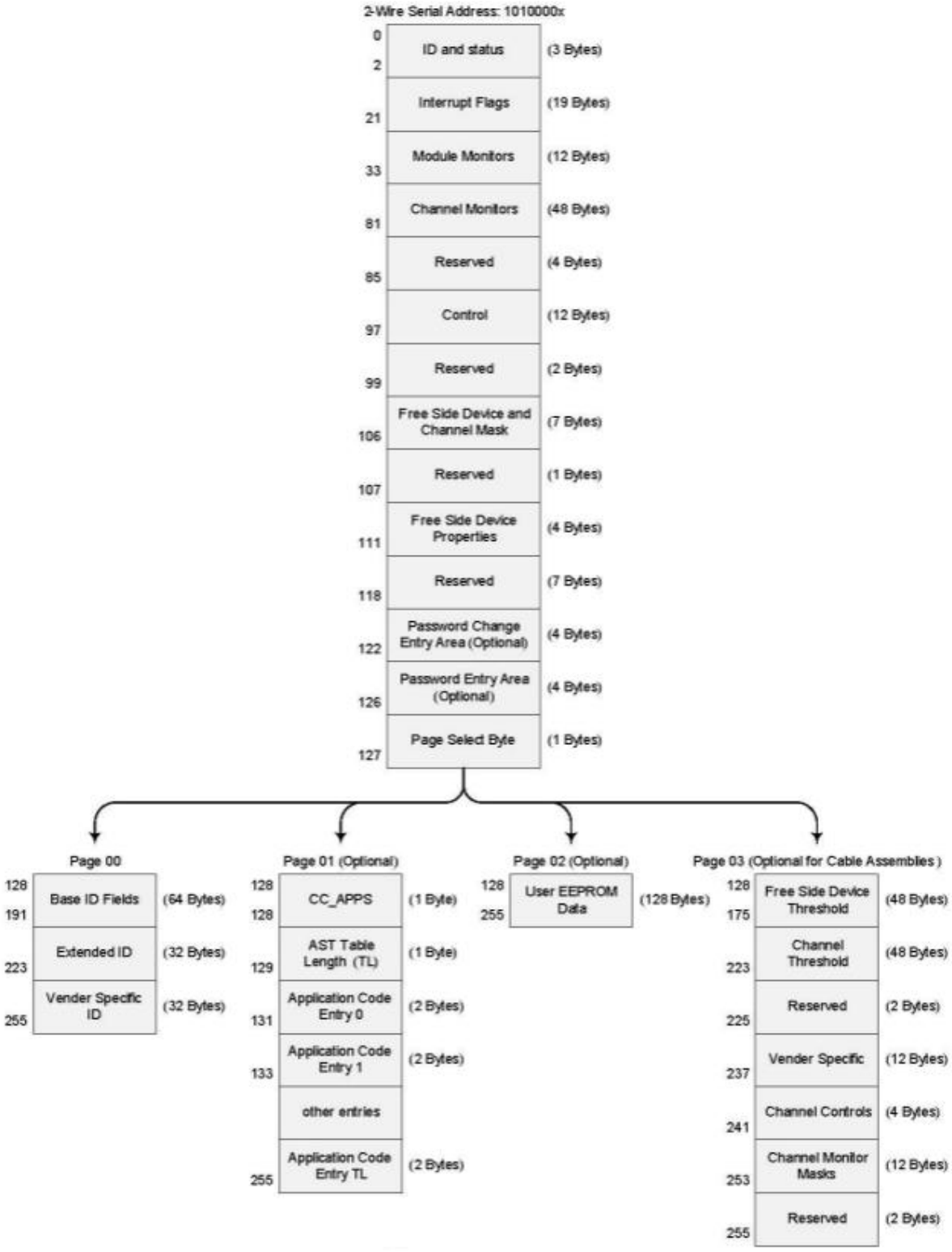


RECOMMENDED INTERFACE CIRCUIT



MEMORY MAP

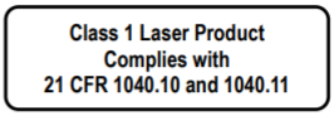
The memory map is structured as a single address and multiple page approaches, according to the QSFP+ SFF-8436 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



EYE SAFETY MARK

The Single-mode transceiver is a class 1 laser product. It complies with EN 60825-1 and FDA 21 CFR 1040.10 and 1040.11. In order to meet laser safety requirements, the transceiver shall be operated within the Absolute Maximum Ratings.

Required Mark



[Caution]

All adjustments have been done at the factory before the shipment of the devices. No maintenance and user serviceable part is required. Tampering with and modifying the performance of the device will result in voided product warranty.

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50.

ADDITIONAL NOTES

- Avoid eye or skin exposure to laser radiations.
- The device is sensitive to electro-static discharge (ESD). The device should be handled with ESD proof tools. To assemble the device on PCB, proper grounding is required to prevent ESD.
- Specifications are subject to change without notice.

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