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**Data Sheet**
Rev 01.1220

# 40GBASE-SR4 850nm MMF 300m QSFP+ Optical Transceiver with Duplex MPO Connector

## 40GMSRSFPC

### DESCRIPTION

The 40GMSRSFPC QSFP+ 40GBASE-SR4 Transceiver product is a new high-speed module with a MPO connector. This interconnecting module offers 4 channels and maximum bandwidth of 40Gbps. The TRxs utilize multimode fiber with 850-nm VCSELs and PIN PDs. This module provides high performance and excellent efficiency in the optical communication.

### FEATURES

- Compliant with 40G Ethernet IEEE 802.3ba 40GBASE-SR4 standards
- QSFP footprint (Quad small form-factor, pluggable)
- Low power dissipation < 1.5W
- Full Digital Diagnostics Monitor Interface
- 0 to 70°C case temperature operating range
- Hot pluggable electrical interface
- RoHS-6 Compliant
- Up to 100m over OM3 fiber
- Up to 150m over OM4 fiber

### APPLICATIONS

- 40GBASE-SR4 Ethernet links
- Infiniband QDR, DDR & SDR interconnects
- Client-side 40G Telecom connections
- 4G/8G/10G Fiber Channel
- SATA/SAS Storage

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Storage Temperature | $T_S$ | -40 | 85 | °C |
| Supply Voltage | $V_{CC}$ | -0.5 | 3.6 | V |
| Data Input Voltage – Single Ended | | -0.5 | $V_{CC}$+0.5 | V |
| Relative Humidity | RH | 5 | 85 | % |
| Rx Optical Damage Threshold / Lane | DT | 3.4 | | dBm |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| Case Operating Temperature | $T_C$ | 0 | 40 | 70 | °C |
| 3.3V Power Supply Voltage | $V_{CC}$ | 3.135 | 3.3 | 3.465 | V |
| Signal Rate per Channel | B | | 10.3125 | | Gb/s |
| Control Input Voltage High | Vih | 2 | | $V_{CC}$+0.3 | V |
| Control Input Voltage Low | Vil | -0.3 | | 0.8 | V |
| Two Wire Serial (TWS) Interface Clock Rate | | | | 400 | KHz |
| Receiver Differential Data Output Load | $Z_d$ | | 100 | | Ohms |
| Fiber Length: 500MHz z•km 50µm MMF (OM2) | | 0.5 | | 30 | m |
| Fiber Length: 2000MHz z•km 50µm MMF (OM3) | | 0.5 | | 100 | m |
| Fiber Length: 4700MHz z•km 50µm MMF (OM4) | | 0.5 | | 150 | m |

### TRANSMITTER ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Power Consumption | P | | | 1.5 | W | |
| Power Supply Current | $I_{CC}$ | | | 420 | mA | |
| TRx Power-On Initialization Time | | | | 2000 | ms | Note 1 |
| Data Input Differential Peak-to-Peak Voltage Swing | $V_{DIFF}$ | 200 | | 1200 | mVpp | |
| Differential Input Return Loss | Per IEEE 802.3ba, Section 86A.4.1.1 | | | | dB | Note 2 |
| Differential to Common Mode Input Return Loss | | 10 | | | dB | Note 2 |
| J2 Jitter Tolerance | Jt2 | 0.17 | | | UI | |
| J9 Jitter Tolerance | Jt9 | 0.29 | | | UI | |
| Eye Mask Coordinates:<br>X1, X2; Y1, Y2 | | Specification Value<br>0.11, 0.31; 95, 350 | | | UI; mV | Note 3 |

### RECEIVER ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT | NOTES |
|---|---|---|---|---|---|---|
| Data Output Differential Peak-to-Peak Voltage Swing | | 200 | | 900 | mVpp | Note 4 |
| Output Transition Time 20% to 80% | Tr, Tf | 28 | | | ps | |
| Differential Output Return Loss | Per IEEE 802.3ba, Section 86A.4.2.1 | | | | dB | Note 2 |
| Common Mode Output Return Loss | Per IEEE 802.3ba, Section 86A.4.2.2 | | | | dB | Note 2 |
| Output Total Jitter | | | | 62 | ps | |
| J2 Jitter Output | Jo2 | | | 0.42 | UI | |
| J9 Jitter Output | Jo9 | | | 0.65 | UI | |
| Eye Mask Coordinates:<br>X1, X2; Y1, Y2 | | Specification Value<br>0.25, 0.5; 150, 425 | | | UI; mV | Note 3 |

**Notes:**

1. "Initialization Time" is the time from when the supply voltages reach and remain above the minimum "Recommended Operating Conditions" to the time when the module enables TWS access. The module at that point is fully functional.
2. 10M to 11.1 GHz according to IEEE 802.3ba specification.
3. Hit ratio= 5 × 10-5 per sample.
4. AC-Coupled with 100Ω differential output impedance.

### TRANSMITTER OPTICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Central Wavelength | λ | 840 | | 860 | nm | |
| Spectral Width – RMS | Δλ | | | 0.65 | nm | |
| Average Output Power, each lane | PO | -7.6 | | 2.4 | dBm | |
| Output Optical Modulation Amplitude, per lane | OMA | -5.6 | | | dBm | |
| Difference in Power between any Two Lanes in OMA | | | | 4.0 | dB | |
| Transmitter and Dispersion Penalty (TDP), each lane | TDP | | | 3.5 | dB | |
| Optical Extinction Ratio | ER | 3 | | | dB | |
| Disabled Output Optical Power | PO_OFF | | | -30 | dBm | |
| Eye Mask Coordinates: X1, X2, X3; Y1, Y2, Y3 | | 0.23, 0.34, 0.43; 0.27, 0.35, 0.4 | | | UI | Note 1 |

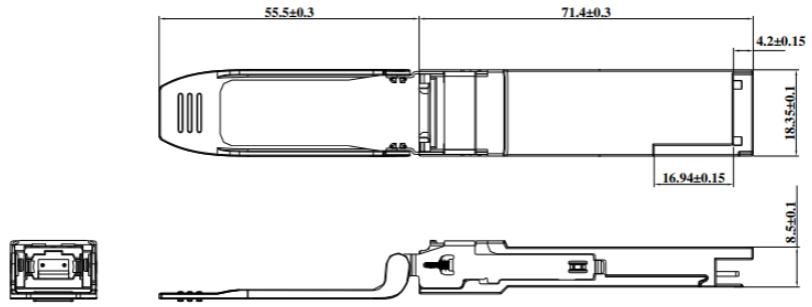
### RECEIVER OPTICAL CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Central Wavelength, each lane | λ | 840 | 850 | 860 | nm | |
| Damage Threshold | | 3.4 | | | dBm | |
| Average Power at Receiver Input, each lane | $P_{IN}$ | -9.5 | | 2.4 | dBm | |
| Stressed Sensitivity (OMA) | | | | -5.4 | dBm | Note 2 |
| Non-Stressed Sensitivity (Average), each lane | | | | -7.5 | dBm | Note 2 |
| LOS Assert | $P_A$ | -30 | | | dBm | |
| LOS De-Assert | $P_D$ | | | -9 | dBm | |
| LOS Hysteresis | | 0.5 | | | dB | |

**Notes:**

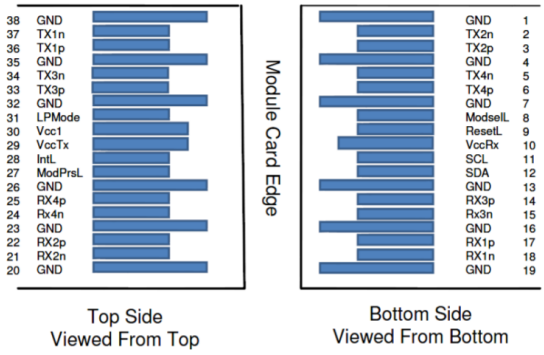
1. Hit ratio= 5 × 10-5 per sample.
2. Measured with 10.3125-Gbps of PRBS-31 at 10-12 BER.

## DIMENSIONS




DIMENSIONS ARE IN MILLIMETERS

## PAD ASSIGNMENT AND DESCRIPTION




Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

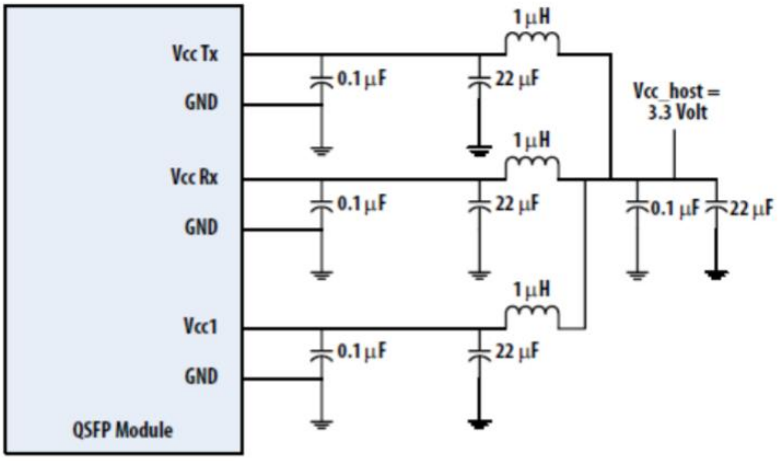
| PIN | LOGIC | SYMBOL | DESCRIPTION | PLUG SEQUENCE | NOTE |
|---|---|---|---|---|---|
| *1* | | GND | Ground | 1 | Note 1 |
| *2* | CML-I | Tx2n | Transmitter Inverted Data Input | 3 | |
| *3* | CML-I | Tx2p | Transmitter Non-Inverted Data Input | 3 | |
| *4* | | GND | Ground | 1 | Note 1 |
| *5* | CML-I | Tx4n | Transmitter Inverted Data Input | 3 | |
| *6* | CML-I | Tx4p | Transmitter Non-Inverted Data Input | 3 | |
| *7* | | GND | Ground | 1 | Note 1 |
| *8* | LVTTL-I | ModSelL | Module Select | 3 | |
| *9* | LVTTL-I | ResetL | Module Reset | 3 | |
| *10* | | Vcc Rx | +3.3V Power Supply Receiver | 2 | Note 2 |
| *11* | LVCMOS-I/O | SCL | 2-wire serial interface clock | 3 | |
| *12* | LVCMOS-I/O | SDA | 2-wire serial interface data | 3 | |
| *13* | | GND | Ground | 1 | Note 2 |
| *14* | CML-O | Rx3p | Receiver Non- Inverted Data Output | 3 | |
| *15* | CML-O | Rx3n | Receiver Inverted Data Output | 3 | |
| *16* | | GND | Ground | 1 | Note 1 |
| *17* | CML-O | Rx1p | Receiver Non- Inverted Data Output | 3 | |
| *18* | CML-O | Rx1n | Receiver Inverted Data Output | 3 | |
| *19* | | GND | Ground | 1 | Note 1 |
| *20* | | GND | Ground | 1 | Note 1 |
| *21* | CML-O | Rx2n | Receiver Inverted Data Output | 3 | |

| | | | | | |
|---|---|---|---|---|---|
| *22* | CML-O | Rx2P | Receiver Non- Inverted Data Output | 3 | |
| *23* | Logic | GND | Ground | 1 | Note 1 |
| *24* | CML-O | Rx4n | Receiver Inverted Data Output | 3 | |
| *25* | CML-O | Rx4p | Receiver Non- Inverted Data Output | 3 | |
| *26* | | GND | Ground | 1 | Note 1 |
| *27* | LVTTL-O | ModPrsL | Module Present | 3 | |
| *28* | LVTTL-O | IntL | Interrupt | 3 | |
| *29* | LVCMOS-I/O | Vcc Tx | +3.3V Power Supply transmitter | 2 | Note 2 |
| *30* | | Vcc1 | +3.3V Power Supply | 2 | Note 2 |
| *31* | LVTTL-I | LPMode | Low Power Mode | 3 | |
| *32* | | GND | Ground | 1 | Note 1 |
| *33* | CML-I | Tx3p | Transmitter Non- Inverted Data Input | 3 | |
| *34* | CML-I | Tx3n | Transmitter Inverted Data Input | 3 | |
| *35* | | GND | Ground | 1 | Note 1 |
| *36* | CML-I | Tx1p | Transmitter Non- Inverted Data Input | 3 | |
| *37* | CML-I | Tx1n | Transmitter Inverted Data Input | 3 | |
| *38* | | GND | Ground | 1 | Note 1 |

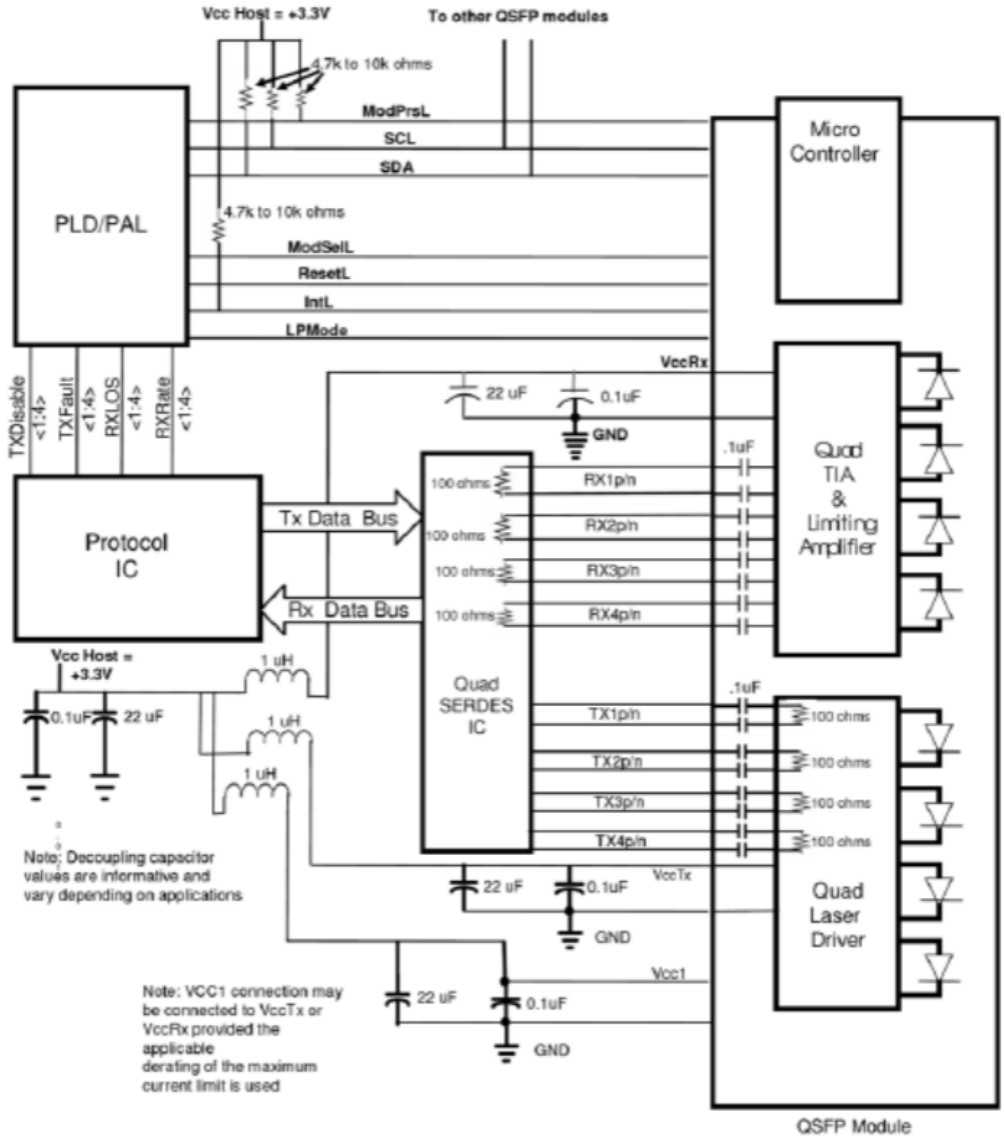
**Note 1:** GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

**Note 2:** Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

## HOST BOARD POWER SUPPLY CIRCUIT

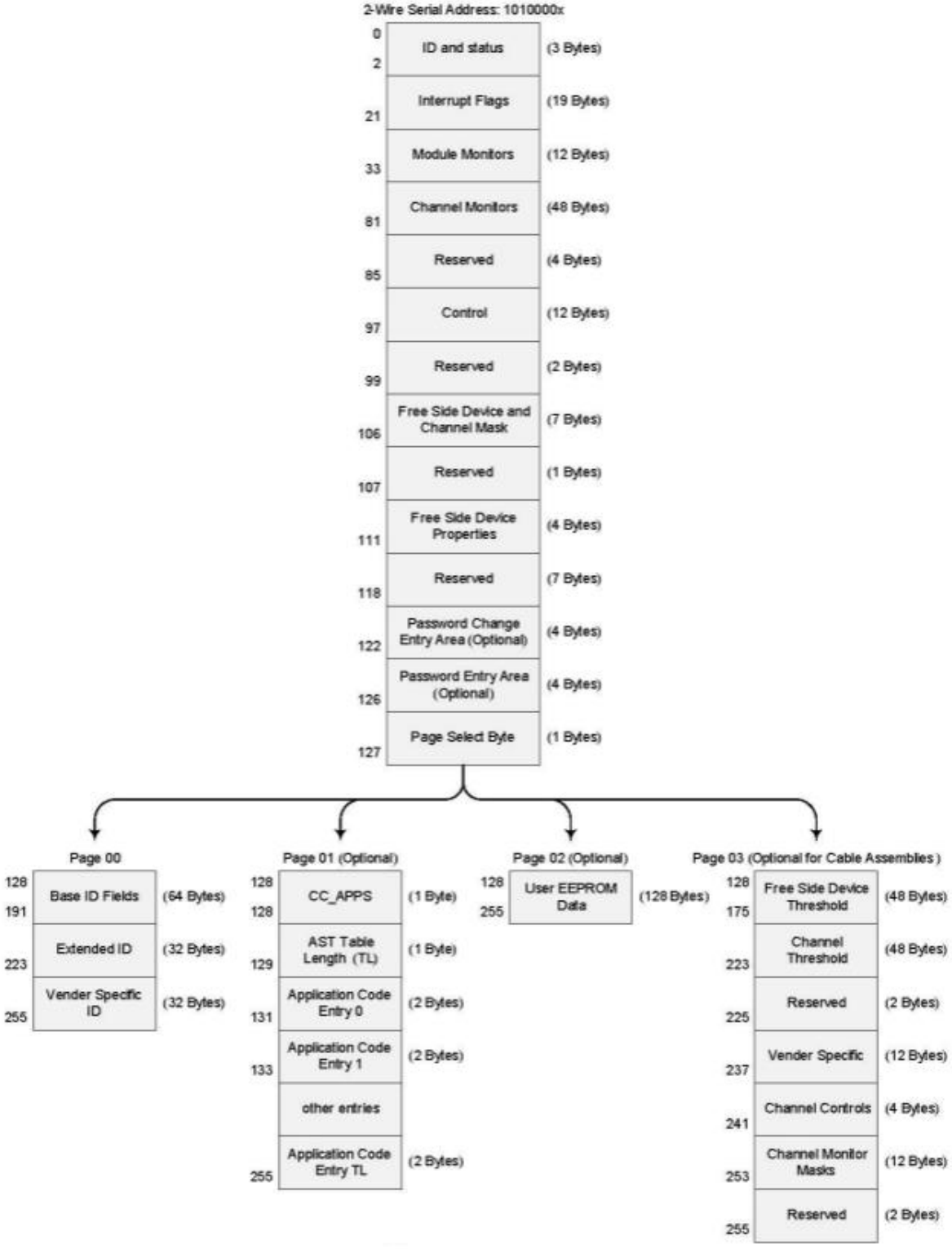


## RECOMMENDED INTERFACE CIRCUIT



## MEMORY MAP

The memory map is structured as a single address and multiple page approaches, according to the QSFP+ SFF-8436 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



## ADDITIONAL NOTES

- Avoid eye or skin exposure to laser radiations.
- The device is sensitive to electro-static discharge (ESD). The device should be handled with ESD proof tools. To assemble the device on PCB, proper grounding is required to prevent ESD.
- Specifications are subject to change without notice.

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