



# 100GBASE-CWDM4 SMF 2km 1310nm CWDM QSFP28 Optical Transceiver with Duplex LC Connector

## 100GCWDMSPCL



### DESCRIPTION

The 100GCWDMSPCL QSFP28 transceiver modules are designed for use in 100 Gigabit Ethernet links on up to 2 km of single mode fiber. They are compliant with the QSFP28 MSA, CWDM4 MSA and portions of IEEE P802.3bm. Digital diagnostics functions are available via the I2C interface, as specified by the QSFP28 MSA.

### FEATURES

- Hot-pluggable QSFP28 form factor
- Power dissipation < 3.5W
- Single 3.3V power supply
- Loss budget of 5 dB on up to 2km of SMF [with KR4 FEC]
- RoHS-6 Compliant (lead-free)
- Case Temperature Operating Range: 0°C to 70°C
- 4x25 Gb/s CWDM transmitter
- 4x25G retimed electrical interface
- Duplex LC receptacle
- I2C management interface

### APPLICATION

- Ethernet Switch
- Data Center Backbone
- 100GBASE Ethernet CWDM4

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Storage Temperature	T <sub>s</sub>	-20	85	°C
3.3V Power Supply Voltage	V <sub>CC</sub>	-0.5	3.6	V
Relative Humidity	RH	5	85	%

**Note:** Exceeding these values may cause permanent damage. Function operation under these conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Case Operating Temperature	T <sub>c</sub>	0		70	°C
3.3V Power Supply Voltage	V <sub>cc</sub>	3.14	3.3	3.46	V
Power Dissipation				3.5	W

**TRANSMITTER OPTICAL CHARACTERISTICS**

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Operating Data Rate	DR		25.78125		Gbps
Total Average Launch Power	P <sub>t</sub>			8.5	dBm
Average Launch Power, per Lane		-6.5		2.5	dBm
Extinction Ratio	ER	3.5			dB
Optical Modulation Amplitude, per lane	P <sub>oma</sub>	-4		2.5	dBm
Transmitter Dispersion Penalty, each lane	TDP			3	dB
Lane Center Wavelength	L0	1264.5		1277.5	nm
	L1	1284.5		1297.5	
	L2	1304.5		1317.5	
	L3	1324.5		1337.5	
Side Mode Suppression	SMSR	-30			dB
Transmitter Reflectance	R <sub>T</sub>			-12	dB
Disable Output Power	P <sub>o_off</sub>			-30	dBm
Output Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}			

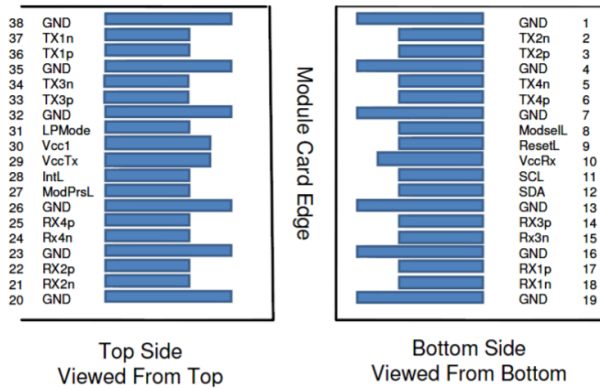
**RECEIVER OPTICAL CHARACTERISTICS**

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Receive Saturation (OMA), per lane	R <sub>max</sub>	2.5			dBm
Damage Threshold, per lane		3.5			dBm
Average Receiver Power, each lane		-11.5		2.5	dBm
Unstressed Receiver Sensitivity (OMA), per lane	R <sub>xsens</sub>			-10	dBm
Stressed Receiver Sensitivity (OMA), per lane	SRS			-7.3	dBm
Receiver Reflectance	R <sub>R</sub>			-26.0	dB
Conditions of stressed receiver sensitivity test:					
SRS eye mask definition {X1, X2, X3, Y1, Y2, Y3}		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}			
LOS De-Assert	LOSD			-12	dBm
LOS Assert	LOSA	-24			dBm
LOS Hysteresis			1.5		dB

**ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Data Rate, per lane			25.78125		Gbps
LP Mode/Reset/Modsell	V <sub>IL</sub>	-0.3		0.8	V
LP Mode/Reset/Modsell	V <sub>IH</sub>	2		V <sub>cc</sub> +0.3	V
ModPrsL/IntL	V <sub>OL</sub>	0		0.4	V
ModPrsL/IntL	V <sub>OH</sub>	V <sub>cc</sub> -0.5		V <sub>cc</sub> +0.3	V

**PAD ASSIGNMENT AND DESCRIPTION**

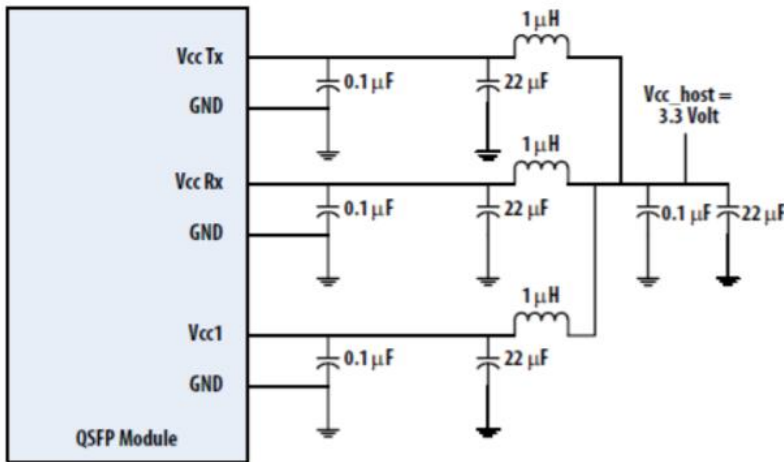


PIN	LOGIC	SYMBOL	DESCRIPTION	PLUG SEQUENCE	NOTE
1		GND	Ground	1	Note 1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	Note 1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	Note 1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	Note 2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	Note 2
14	CML-O	Rx3p	Receiver Non- Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	Note 1
17	CML-O	Rx1p	Receiver Non- Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	Note 1
20		GND	Ground	1	Note 1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2P	Receiver Non- Inverted Data Output	3	
23		GND	Ground	1	Note 1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non- Inverted Data Output	3	
26		GND	Ground	1	Note 1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29	LVC MOS-I/O	Vcc Tx	+3.3V Power Supply transmitter	2	Note 2
30		Vcc1	+3.3V Power Supply	2	Note 2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	Note 1
33	CML-I	Tx3p	Transmitter Non- Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	Note 1
36	CML-I	Tx1p	Transmitter Non- Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	Note 1

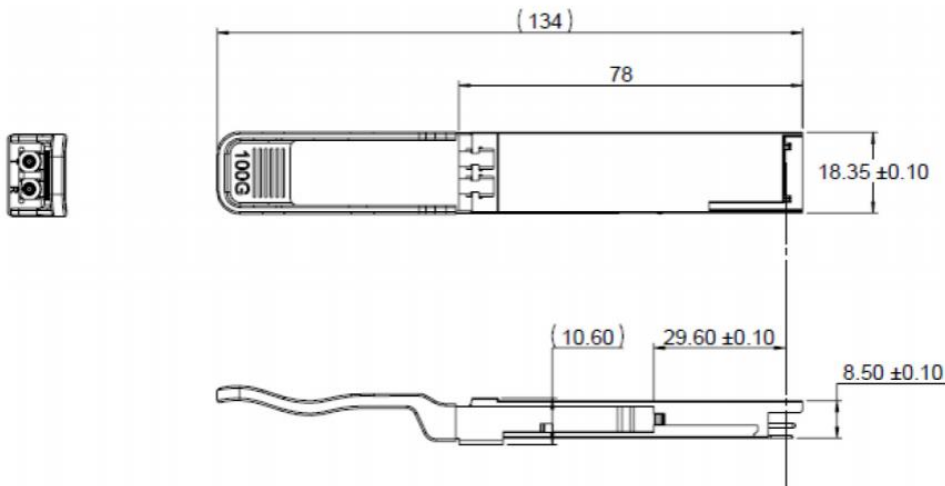
**Note 1:** GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

**Note 2:** Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.

**HOST BOARD POWER SUPPLY CIRCUIT**



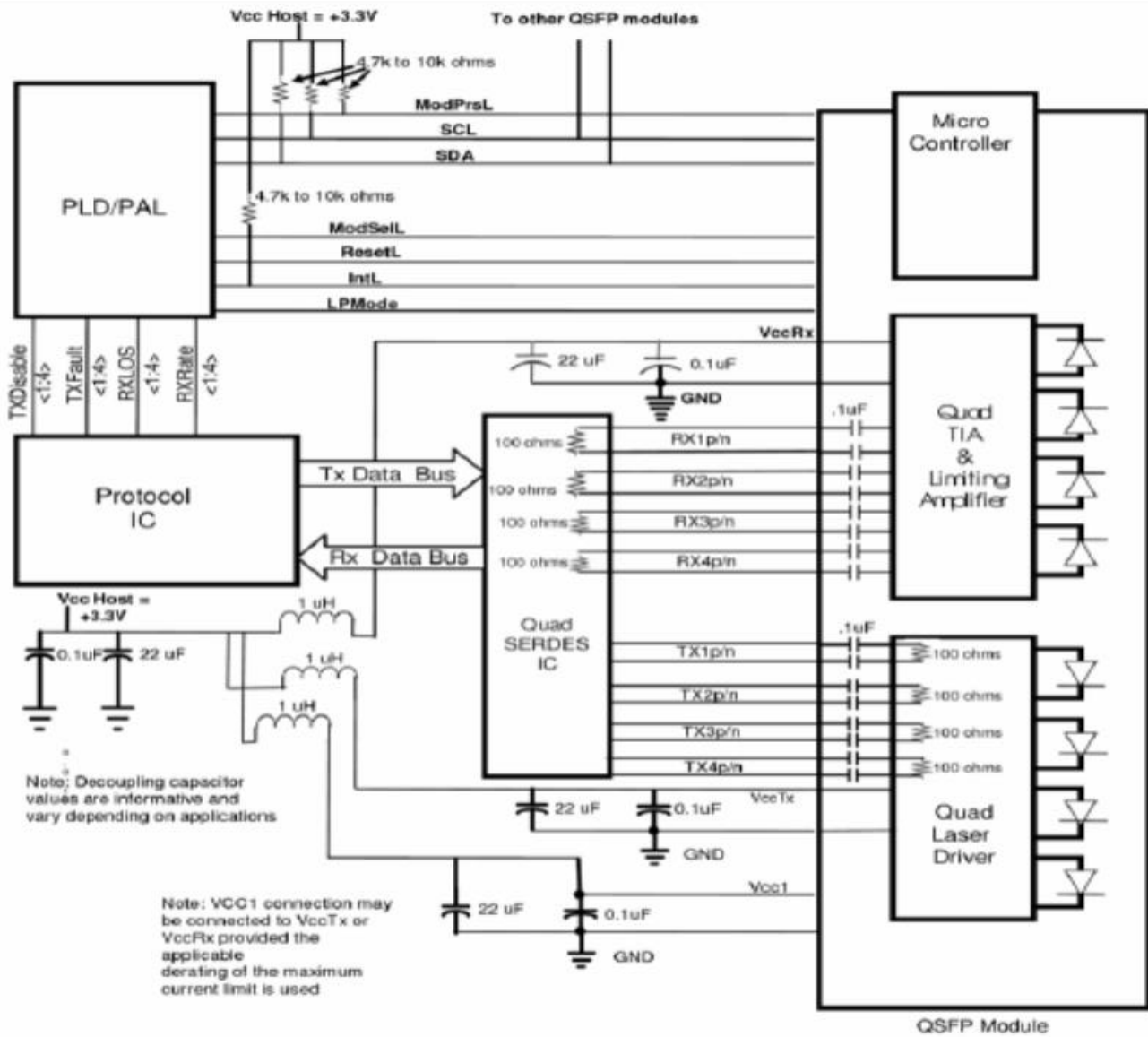
**DIMENSIONS**



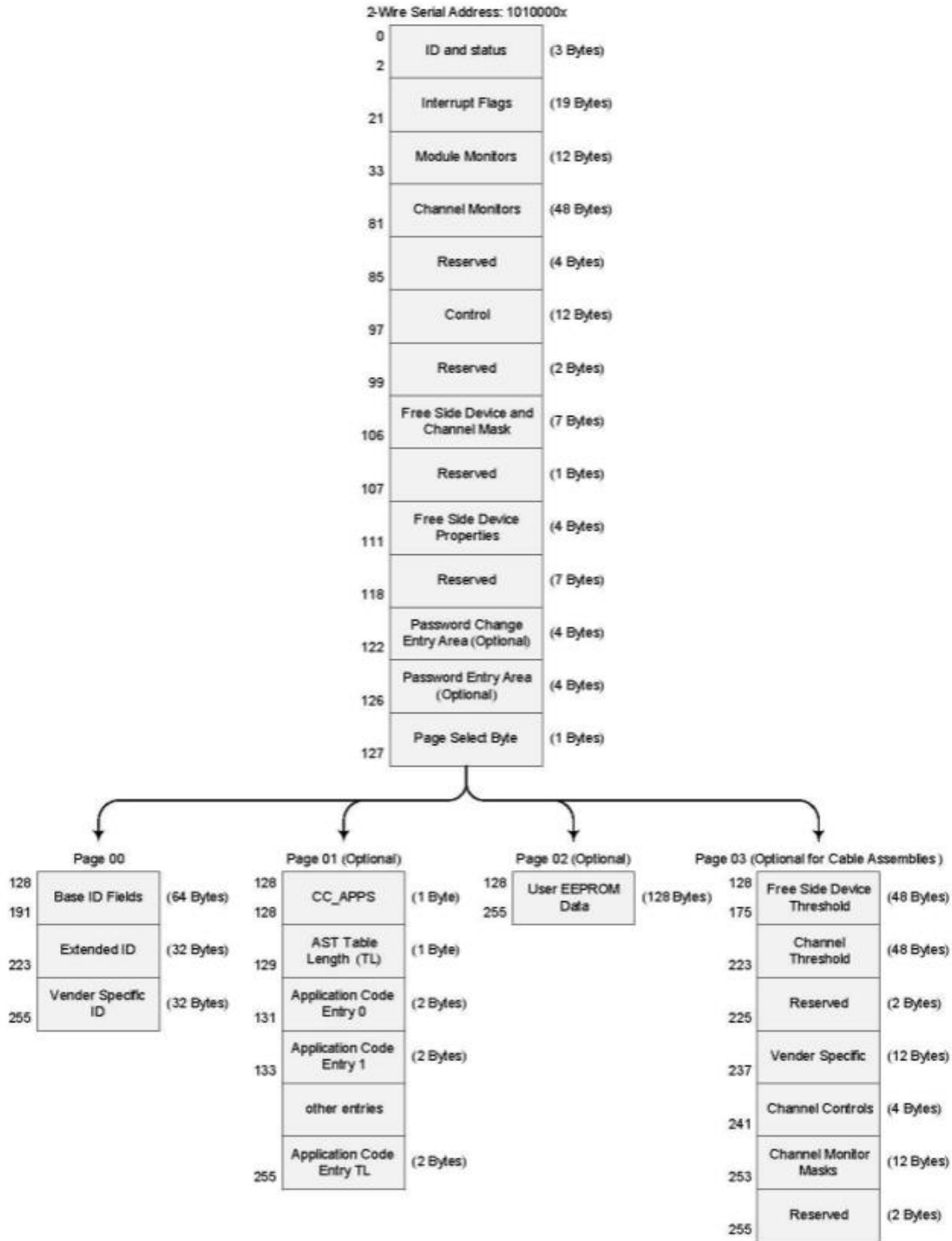
Unit: mm

All Dimensions are ±0.20mm Unless Otherwise Specified

RECOMMENDED INTERFACE CIRCUIT



MEMORY MAP



**ADDITIONAL NOTES**

- Avoid eye or skin exposure to laser radiations.
- The device is sensitive to electro-static discharge (ESD). The device should be handled with ESD proof tools. To assemble the device on PCB, proper grounding is required to prevent ESD.
- Specifications are subject to change without notice.



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