



155Mbps 1470nm~1610nm SMF 35dB CWDM 1x9 Optical Transceiver with Duplex ST Connector

CS15xxD-03A-3U-PC-T



DESCRIPTION

The CS15xxD-03A-3U-PC-T duplex 1x9 optical transceivers are high performance, cost effective optical transceiver modules support data rates up to 155Mb/s. They provide 35dB power budget over single mode fiber. There are eight center wavelengths available from 1470nm to 1610nm with 20nm channel spacing.

FEATURES

- Compliant with 155 Mbps ATM and SONET OC-3 SDH STM-1
- Industry standard 1x9 footprint
- ST duplex connector (plastic)
- Single power supply 3.3V
- Differential PECL inputs and outputs
- Compatible with solder and aqueous wash processes
- Class 1 laser product compliant with EN 60825-1
- Input/Output: DC/DC
- Temperature: 0°C to 70°C
- 35dB power budget

APPLICATIONS

- CWDM Network

PRODUCT OVERVIEW

PART NUMBER	WAVELENGTH
CS1547D-03A-3U-PC-T	1470nm
CS1549D-03A-3U-PC-T	1490nm
CS1551D-03A-3U-PC-T	1510nm
CS1553D-03A-3U-PC-T	1530nm
CS1555D-03A-3U-PC-T	1550nm
CS1557D-03A-3U-PC-T	1570nm
CS1559D-03A-3U-PC-T	1590nm
CS1561D-03A-3U-PC-T	1610nm

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T _S	-40	85	°C	
Supply Voltage	V _{CC}	-0.5	4.0	V	
Input Voltage	V _{IN}	-0.5	V _{CC}	V	
Output Current	I _o	-	50	mA	
Operating Current	I _{OP}	-	400	mA	
Soldering Temperature	T _{SOLD}	-	260	°C	10 seconds on leads

OPERATING ENVIRONMENT

PARAMETER	SYMBOL	MIN	MAX	UNIT
Case Operating Temperature	T _C	0	70	°C
Supply Voltage	V _{CC}	3.1	3.5	V

TRANSMITTER ELECTRO-OPTICAL CHARACTERISTICS (V_{CC} = 3.1V to 3.5V, T_C = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Data Rate	B	50	155	200	Mbps	
Output Optical Power 9/125um fiber	P _{out}	0	-	+5	dBm	Average
Extinction Ratio	ER	10	-	-	dB	
Center Wavelength	λ _C	x-5.5	x+1	x+7.5	nm	
Spectral Width (-20dB)	Δλ	-	-	1	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Rise/Fall Time (10~90%)	T _{r,f}	-	1	2	ns	
Output Eye	Compliant with Telcordia GR-253-CORE Issue 3 and ITU-T recommendation G-957					
Power Supply Current	I _{CC}	-	-	180	mA	Note 1
Transmitter Data Input Voltage-High	V _{IH} -V _{CC}	-1.1	-	-0.74	V	Note 2
Transmitter Data Input Voltage-Low	V _{IL} -V _{CC}	-2.0	-	-1.58	V	Note 2
Transmitter Data Input Differential Input Voltage	V _{DIFF}	0.3	-	1.6	V	Note 2

Note 1: Note including the terminations.

Note 2: These inputs are compatible with 10K, 10KH and 100K ECL and PECL input.

RECEIVER ELECTRO-OPTICAL CHARACTERISTICS (V_{CC} = 3.1V to 3.5V, T_C = 0°C to 70°C)

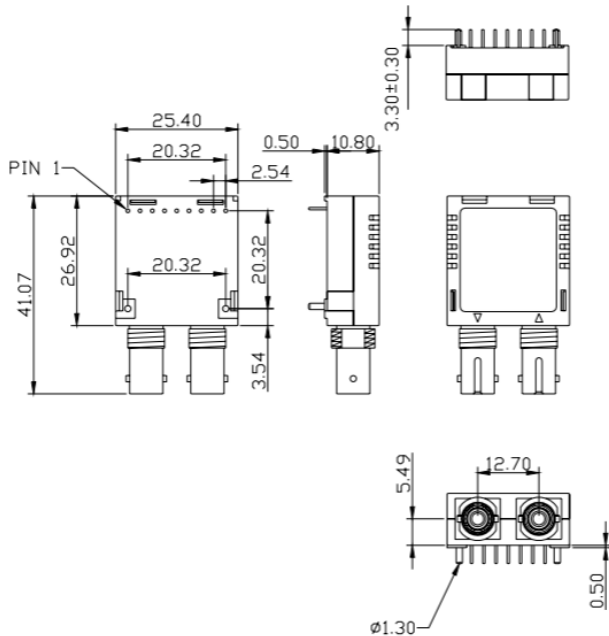
PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Data Rate	B	50	155	200	Mbps	
Optical Input Power-Maximum	P _{IN}	0	-	-	dBm	Note 1
Receiver Input Power-Minimum (Sensitivity)	P _{IN}	-	-	-35	dBm	Note 1
Operating Center Wavelength	λ _C	1260	-	1620	nm	
Signal Detect-Asserted	P _A	-	-	-35	dBm	Average
Signal Detect-Deasserted	P _D	-45	-	-	dBm	Average
Signal Detect-Hysteresis	P _A -P _D	1.0	-	-	dB	
Signal Detect Output Voltage-High	V _{OH} -V _{CC}	-1.1	-	-0.74	V	Note 2
Signal Detect Output Voltage-Low	V _{OL} -V _{CC}	-2.0	-	-1.58	V	Note 2
Power Supply Current	I _{CC}	-	-	100	mA	Note 3
Data Output Rise, Fall time (10~90%)	T _{r,f}	-	1	2	ns	
Data Output Voltage-High	V _{OH} -V _{CC}	-1.1	-	-0.74	V	Note 2
Data Output Voltage-Low	V _{OL} -V _{CC}	-2.0	-	-1.58	V	Note 2

Note 1: The input data is at 155.52 Mbps, 2²³-1 PRBS data pattern with 72 "1"s and 72 "0"s inserted per the ITU-T recommendation G.958 Appendix 1. The receiver is guaranteed to provide output data with Bit Error Rate (BER) better than or equal to 1 × 10⁻¹⁰.

Note 2: These outputs are compatible with 10K, 10KH and 100K ECL and PECL input.

Note 3: The current excludes the output load current.

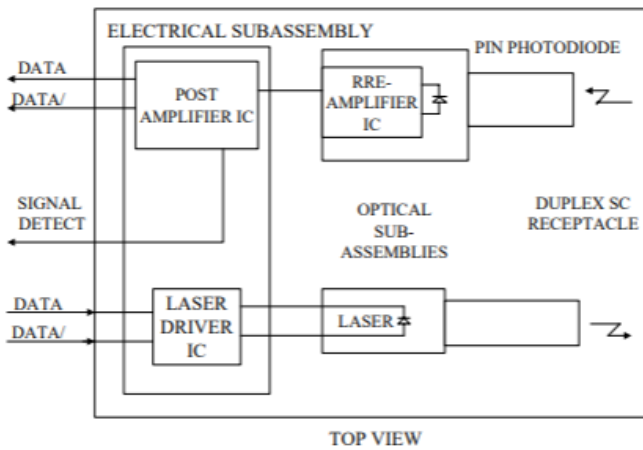
DRAWING DIMENSIONS



ALL DIMENSIONS ARE ±0.20mm UNLESS OTHERWISE SPECIFIED

Unit : mm

BLOCK DIAGRAM OF TRANSCEIVER

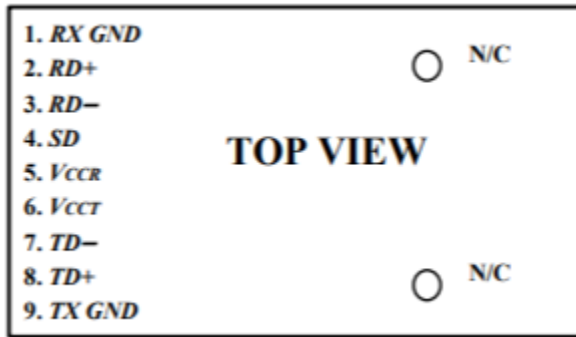


Transmitter Section - The transmitter section consists of a 1550 nm InGaAsP in an eye safe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a LD driver IC which converts differential input PECL logic signals into an analog laser driving current.

Receiver Section - The receiver utilizes an InGaAs PIN photodiode mounted together with a trans-impedance preamplifier IC in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

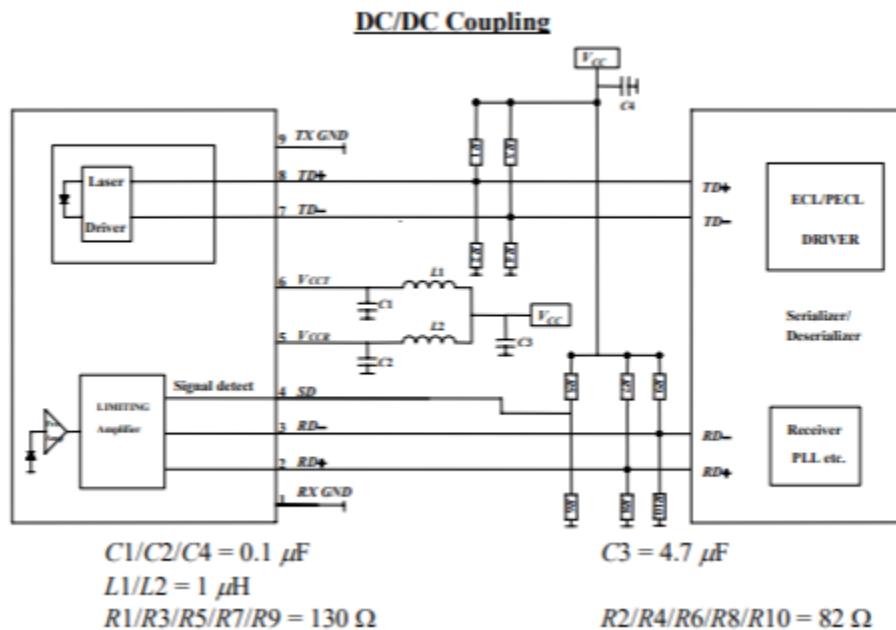
Receiver Signal Detect - Signal Detect is a basic fiber failure indicator. This is a single-ended PECL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 1.0 dB higher than the deassert level.

CONNECTION DIAGRAM



PIN	SYMBOL	DESCRIPTION
1	<i>RX GND</i>	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	<i>RD+</i>	<i>RD+</i> is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
3	<i>RD-</i>	<i>RD-</i> is an open-emitter output circuit . Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
4	<i>SD</i>	Signal Detect. Normal optical input levels to the receiver result in a logic “1” output, V_{OH} , asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic “0” output V_{OL} , deasserted Signal Detect is a single-ended LVPECL output. <i>SD</i> can be terminated with LVPECL techniques via 50 Ω to $V_{CCR} - 2$ V. Alternatively, <i>SD</i> can be loaded with a 180 Ω resistor to <i>RX GND</i> to conserve electrical power with small compromise to signal quality. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
5	V_{CCR}	Receiver Power Supply. Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCR} pin.
6	V_{CCT}	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V_{CCT} pin.
7	<i>TD-</i>	Transmitter Data In-Bar. Terminate this high-speed differential PECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)
8	<i>TD+</i>	Transmitter Data In. Terminate this high-speed differential PECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)
9	<i>TX GND</i>	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.

RECOMMENDED CIRCUIT SCHEMATIC



In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic. When designing the circuit interface, there are a few fundamental guidelines to follow.

- (1) The differential data lines should be treated as 50 Ω Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.
- (2) For the high-speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.
- (3) Multi-layer plane PCB is best for distribution of VCC, returning ground currents, forming transmission lines and shielding. Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.
- (4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress VCC noise over a broad frequency range, this prevents receiver sensitivity degradation due to VCC noise.
- (5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1 μF capacitors and a surface-mount coil inductor for 1 μH inductor. Ferrite beads can be used to replace the coil inductors when using quieter VCC supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the VCC pins of the receiver and transmitter.
- (6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

ADDITIONAL NOTES

- Avoid eye or skin exposure to laser radiations.
- The device is sensitive to electro-static discharge (ESD). The device should be handled with ESD proof tools. To assemble the device on PCB, proper grounding is required to prevent ESD.
- Specifications are subject to change without notice.



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