



155Mbps 1310nm MMF 2km 2x5 SFF Optical Transceiver with Duplex LC Connector

CM13L-03K-3S-Px-L



DESCRIPTION

The CM13L-03K-3S-Px-L duplex 2x5 SFF (Small Form Factor) optical transceivers are high performance, cost effective optical transceiver modules for serial optical data communications application specified for a data rate of 155 Mb/s. The 2x5 SFF transceiver module provides 2km transmission distance over multi-mode fiber at nominal wavelength of 1310nm. The optical transceiver is RoHS compliant.

FEATURES

- RoHS compliant
- Industry standard 2x5 footprint
- LC duplex connector
- Single power supply 3.3V
- Differential LVPECL inputs and outputs
- Compatible with solder and aqueous wash processes
- Class 1 laser product compliant with EN 60825-1
- Input/Output: DC/DC
- Up to 2km over multimode fiber

APPLICATIONS

- Fast Ethernet / OC3

PRODUCT OVERVIEW

PART NUMBER	OPERATING TEMPERATURE
CM13L-03K-3S-PC-L	0°C to 70°C
CM13L-03K-3S-PI-L	-40°C to 85°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T _S	-40	85	°C	
Supply Voltage	V _{CC}	-0.5	4.0	V	
Input Voltage	V _{IN}	-0.5	V _{CC}	V	
Output Current	I _O	-	50	mA	
Operating Current	I _{OP}	-	400	mA	
Soldering Temperature	T _{SOLD}	-	260	°C	10 seconds on leads

OPERATING ENVIRONMENT

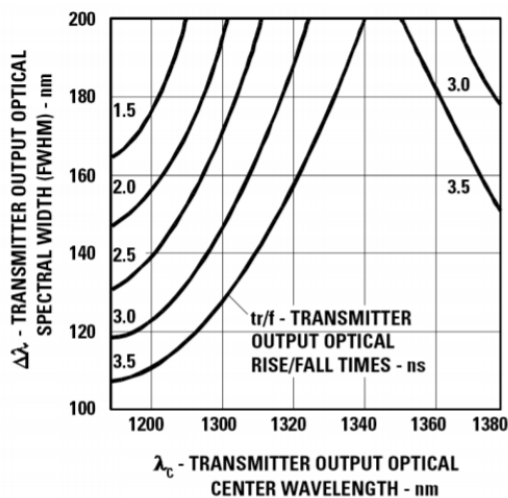
PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Case Operating Temperature	T _C	0	70	°C	CM13L-03K-3S-PC-L
		-40	85		CM13L-03K-3S-PI-L
Supply Voltage	V _{CC}	3.1	3.5	V	
Total Supply Current	I _{CC} (TX+RX)		300	mA	

TRANSMITTER ELECTRO-OPTICAL CHARACTERISTICS (V_{CC} = 3.1V to 3.5V, T_C = 0°C to 70°C, -40°C to 85°C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Data Rate	B	10	155	200	Mbps	
Output Optical Power 62.5/125um fiber	P _{out}	-20	-	-14	dBm	Average
Output Optical Power 50/125um fiber	P _{out}	-23.5	-	-14	dBm	Average
Extinction Ratio	ER	10	-	-	dB	
Center Wavelength	λ _c		Fig 1		nm	
Spectral Width (FWHM)	Δλ		Fig 1		nm	
Rise/Fall Time (10~90%)	T _{r,f}		Fig 1		ns	
Duty Cycle Distortion	DCD			0.6	ns	
Data Dependent Jitter	DDJ			0.6	ns	
Random Jitter	RJ			0.6	ns	
Transmitter Data Input Voltage-High	V _{IH} -V _{CC}	-1.1	-	-0.74	V	Note 1
Transmitter Data Input Voltage-Low	V _{IL} -V _{CC}	-2.0	-	-1.58	V	Note 1

Note 1: These inputs are compatible with 10K, 10KH, and 100K ECL and PECL input.

Fig 1 – LED Spectral Width/Rise, Fall Time/Center Wavelength Limit



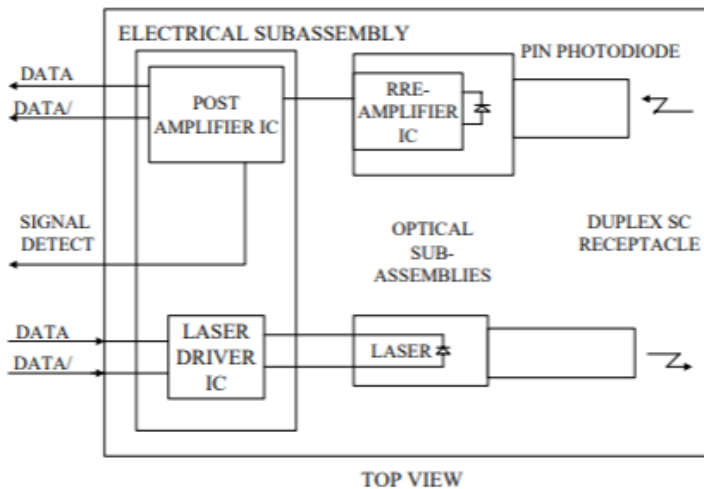
RECEIVER ELECTRO-OPTICAL CHARACTERISTICS ($V_{CC} = 3.1V$ to $3.5V$, $T_C = 0^{\circ}C$ to $70^{\circ}C$, $-40^{\circ}C$ to $85^{\circ}C$)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTES
Data Rate	B	10	155	200	Mbps	
Optical Input Power-Maximum	P_{IN}	-8	-	-	dBm	Note 1
Receiver Input Power-Minimum (Sensitivity)	P_{IN}	-	-	-31	dBm	Note 1
Operating Center Wavelength	λ_C	1260	-	1610	nm	
Signal Detect-Asserted	P_A	-	-	-31	dBm	Average
Signal Detect-Deasserted	P_D	-45	-	-	dBm	Average
Signal Detect-Hysteresis	$P_A - P_D$	1.0	-	-	dB	
Signal Detect Output Voltage-High	$V_{OH} - V_{CC}$	-1.1	-	-0.74	V	Note 2
Signal Detect Output Voltage-Low	$V_{OL} - V_{CC}$	-2.0	-	-1.58	V	Note 2
Data Output Rise, Fall time (10~90%)	$T_{r,f}$	-	-	3	ns	
Data Output Voltage-High	$V_{OH} - V_{CC}$	-1.1	-	-0.74	V	Note 2
Data Output Voltage-Low	$V_{OL} - V_{CC}$	-2.0	-	-1.58	V	Note 2

Note 1: The input data is at 155 Mbps, $2^{23}-1$ PRBS data pattern. The receiver is guaranteed to provide output data with Bit Error Rate (BER) better than or equal to 2.5×10^{-10} .

Note 2: These outputs are compatible with 10K, 10KH and 100K ECL and PECL input.

BLOCK DIAGRAM OF TRANSCEIVER

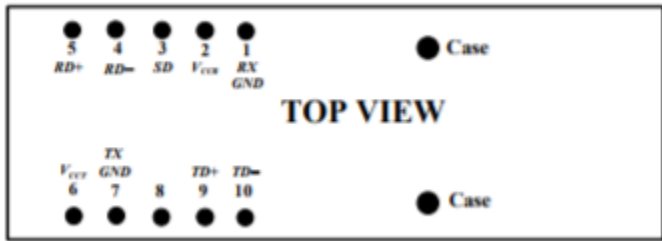


Transmitter Section - The transmitter section consists of a 1310nm InGaAsP LED in an optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a LED driver IC which converts differential input LVPECL logic signals into an analog laser driving current.

Receiver Section - The receiver utilizes an InGaAs PIN photodiode mounted together with a trans-impedance preamplifier IC in an OSA. This OSA is connected to a circuit providing post-amplification quantization, and optical signal detection.

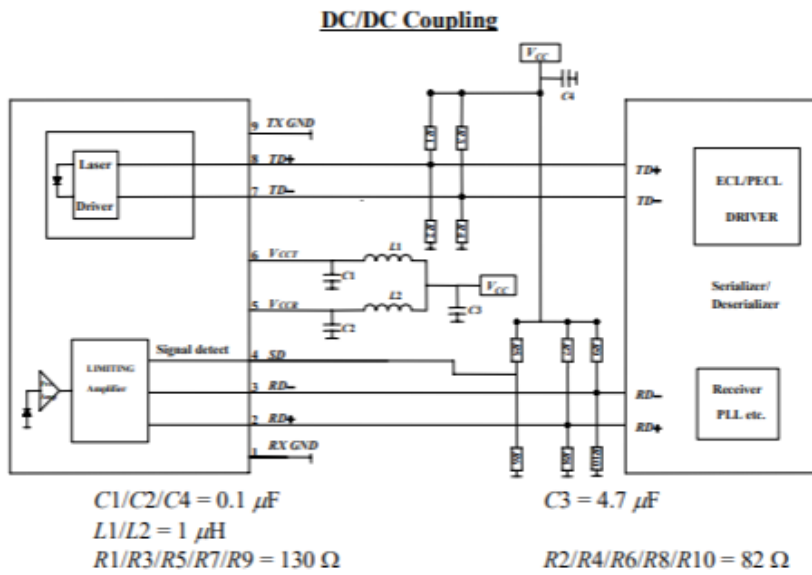
Receiver Signal Detect - Signal Detect is a basic fiber failure indicator. This is a single-ended LVPECL output. As the input optical power is decreased, Signal Detect will switch from high to low (deassert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 1.0 dB higher than the deassert level.

CONNECTION DIAGRAM



PIN	SYMBOL	DESCRIPTION
1	<i>RX GND</i>	Receiver Signal Ground. Directly connect this pin to the receiver ground plane.
2	<i>V_{CCR}</i>	Receiver Power Supply Provide +3.3 Vdc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the <i>V_{CCR}</i> pin.
3	<i>SD</i>	Signal Detect. Normal optical input levels to the receiver result in a logic “1” output, <i>V_{OH}</i> , asserted. Low input optical levels to the receiver result in a fault condition indicated by a logic “0” output <i>V_{OL}</i> , deasserted. Signal Detect is a single-ended LVPECL output. <i>SD</i> can be terminated with LVPECL techniques via 50Ω to <i>V_{CCR}</i> – 2 V. Alternatively, <i>SD</i> can be loaded with a 180 Ω resistor to <i>RX GND</i> to conserve electrical power with small compromise to signal quality. If Signal Detect output is not used, leave it open-circuited. This Signal Detect output can be used to drive a LVPECL input on an upstream circuit, such as, Signal Detect input or Loss of Signal-bar.
4	<i>RD-</i>	<i>RD-</i> is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
5	<i>RD+</i>	<i>RD+</i> is an open-emitter output circuit. Terminate this high-speed differential LVPECL output with standard LVPECL techniques at the follow-on device input pin. (See recommended circuit schematic)
6	<i>V_{CCT}</i>	Transmitter Power Supply. Provide +3.3 Vdc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the <i>V_{CCT}</i> pin.
7	<i>TX GND</i>	Transmitter Signal Ground. Directly connect this pin to the transmitter signal ground plane. Directly connect this pin to the transmitter ground plane.
8	<i>NC</i>	Not Connected. Internal not connected
9	<i>TD+</i>	Transmitter Data In. Terminate this high-speed differential LVPECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)
10	<i>TD-</i>	Transmitter Data In-Bar. Terminate this high-speed differential LVPECL input with standard LVPECL techniques at the transmitter input pin. (See recommended circuit schematic)

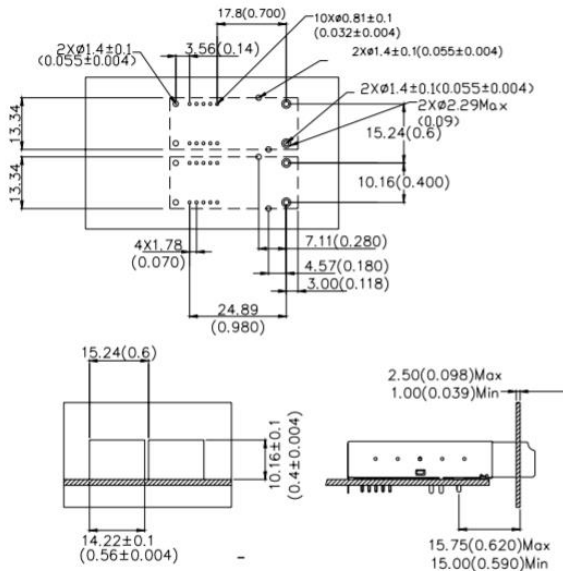
RECOMMENDED CIRCUIT SCHEMATIC



In order to get proper functionality, a recommended circuit is provided in above recommended circuit schematic. When designing the circuit interface, there are a few fundamental guidelines to follow.

- (1) The differential data lines should be treated as 50 Ω Micro strip or strip line transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length.
- (2) For the high-speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents which will cause distortion in the signal.
- (3) Multi-layer plane PCB is best for distribution of VCC, returning ground currents, forming transmission lines and shielding. Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit.
- (4) A separate proper power supply filter circuits shown in Figure for the transmitter and receiver sections. These filter circuits suppress Vcc noise over a broad frequency range, this prevents receiver sensitivity degradation due to VCC noise.
- (5) Surface-mount components are recommended. Use ceramic bypass capacitors for the 0.1 μF capacitors and a surface-mount coil inductor for 1 μH inductor. Ferrite beads can be used to replace the coil inductors when using quieter VCC supplies, but a coil inductor is recommended over a ferrite bead. All power supply components need to be placed physically next to the VCC pins of the receiver and transmitter.
- (6) Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

RECOMMENDED BOARD LAYOUT HOLE PATTERN

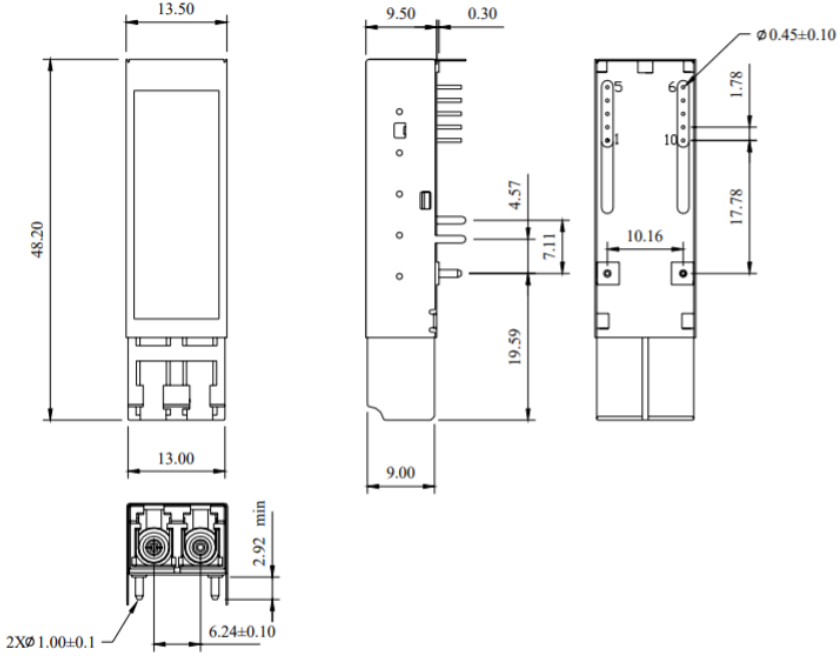


Unit : mm(inches)

This transceiver is compatible with industry standard wave or hand solder processes. After wash process, all moisture must be completely removed from the module. The transceiver is supplied with a process plug to prevent contamination during wave solder and aqueous rinse as well as during handling, shipping or storage.

Solder fluxes should be water-soluble, organic solder fluxes. Recommended cleaning and degreasing chemicals for these transceivers are alcohol's (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing.

DRAWING DIMENSIONS



ALL DIMENSIONS ARE±0.20mm UNLESS OTHERWISE SPECIFIED

Unit : mm

EYE SAFETY MARK

The multi-mode transceiver is a class 1 LED product. It complies with EN 60825-1 and FDA 21 CFR 1040.10 and 1040.11. In order to meet laser safety requirements, the transceiver shall be operated within the Absolute Maximum Ratings.

[Caution] All adjustments have been done at the factory before the shipment of the devices. No maintenance and user serviceable part is required. Tampering with and modifying the performance of the device will result in voided product warranty.

ADDITIONAL NOTES

- Avoid eye or skin exposure to laser radiations.
- The device is sensitive to electro-static discharge (ESD). The device should be handled with ESD proof tools. To assemble the device on PCB, proper grounding is required to prevent ESD.
- Specifications are subject to change without notice.



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